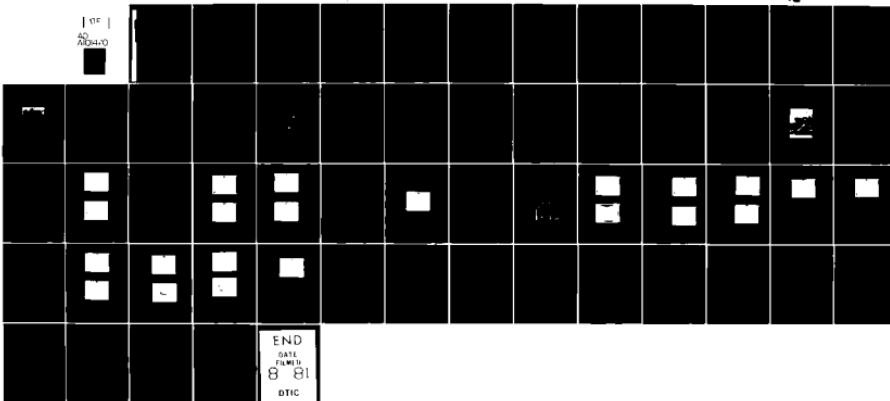


AD-A101 470 VARIAN ASSOCIATES INC PALO ALTO CA SOLID STATE LAB F/6 9/1  
CONTINUATION OF STUDY OF HETEROJUNCTION GATE GAAS FIELD EFFECT --ETC  
MAY 81 T J MALONEY N00173-80-C-0179  
NL

UNCLASSIFIED

| 9F |  
AO  
AD440



END  
SALE  
TJ MARCH  
8 81  
DTIC

DTIC FILE COPY

AD A101470

LEVEL

9

CONTINUATION OF STUDY OF HETEROJUNCTION GATE  
GaAs FIELD EFFECT TRANSISTORS

FINAL REPORT

Contract No. N00173-80-C-0179

Prepared for:

Naval Research Laboratory  
Washington, DC 20375

Prepared by:

T. J. Maloney

Varian Associates, Inc.  
Solid State Laboratory  
Palo Alto, CA 94303

DISSEMINATION COMMENT A	
A <sub>1</sub>	Approved for release; Distribution Unlimited

JUL 1 1981

H

816 22 072

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM	
1 REPORT NUMBER	2 GOVT ACCESSION NO.	3 RECIPIENT'S CATALOG NUMBER	
	AD-A202470		
4 TITLE (and Subtitle)	5. TYPE OF REPORT & PERIOD COVERED		
Continuation of Study of Heterojunction Gate GaAs Field Effect Transistors	9	Final Report May 1980 - May 1981	
7 AUTHOR(s)	6. PERFORMING ORG. REPORT NUMBER		
10 J. J. Maloney Timothy	15	N00173-80-C-0179	
11 PERFORMING ORGANIZATION NAME AND ADDRESS	8. CONTRACT OR GRANT NUMBER(S)		
Varian Associates, Inc. 611 Hansen Way Palo Alto, CA 94303	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS		
11 CONTROLLING OFFICE NAME AND ADDRESS	12. REPORT DATE		
Naval Research Laboratory Washington, D.C. 20375	11	May 1981	
14 MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office)	13. NUMBER OF PAGES		
	12	58	
16 DISTRIBUTION STATEMENT (of this Report)	15. SECURITY CLASS (of this report)		
<p style="text-align: center;"><b>DISTRIBUTION STATEMENT A</b></p> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr><td>A.</td></tr> </table>			A.
A.			
17 DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)			
18 SUPPLEMENTARY NOTES			
19 KEY WORDS /Continue on reverse side if necessary and identify by block number)			
Normally-off GaAs FETs	AlGaAs heterojunction		
Normally-on GaAs FETs	Microwave FETs		
Heterojunction FETs	Organometallic epitaxy		
	Molecular beam epitaxy		
20 ABSTRACT (Continue on reverse side if necessary and identify by block number)			
AlGaAs/GaAs heterojunction gate GaAs FETs have been fabricated with molecular beam epitaxy (MBE) and organometallic vapor phase epitaxy (OM-VPE), which allow for enhanced uniformity and reproducibility. The best results were obtained with MBE n-GaAs active layers and OM-VPE gate layers of p-AlGaAs and p <sup>+</sup> -GaAs. Process steps such as a plasma ash and <u>in situ</u> heat cleaning of the mesa-etched layer before OM-VPE gate growth must be taken in order to ensure that the interface is clean and free of carbon contamination.			

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 68 IS OBSOLETE

UNCLASSIFIED 409970 v1  
SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

## UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE(When Data Entered)

Moreover, a very thin (200 Å) p<sup>+</sup>-GaAs layer between the n-GaAs channel and the p<sup>+</sup>-AlGaAs helps to isolate the actual p<sup>+</sup>n gate junction from oxygen that is gettered into AlGaAs grown by OM-VPE. C-V measurements indicate a 1.3V built-in voltage for this junction, while forward I-V characteristics give a nonideality factor n = 2 and are similar to those of a GaAs p<sup>+</sup>n junction. Thus the electrical characteristics of the heterojunction are retained, along with the advantages of selective undercut etching and self-aligned metal.

Since normally-off HJFETs are desired for direct coupling of logic circuits, control of threshold voltage is very important. Although HJFETs with record high saturation currents were produced with buffered active layers grown by both chloride transport VPE and MBE, extremely good threshold voltage control (variations of 0.1-0.2V over a 1-cm<sup>2</sup> wafer) was achieved with MBE. Saturation currents for normally-off HJFETs followed a square law and were the highest on record, greater than 50 μA/μm<sup>2</sup> for 3 x 300 μm and 1 x 300 μm gate devices. Pt-Au gate metal is especially useful for achieving self-aligned, undercut-etched 1-μm gate devices with low gate resistance. Results are discussed in the light of various process alternatives for GaAs digital ICs, and possible future developments for the HJFET are outlined.

Accesision For	
NTIS GRAZI	<input checked="" type="checkbox"/>
NDIA TAB	<input type="checkbox"/>
Continued	<input type="checkbox"/>
Classification	<input type="checkbox"/>
<i>letter on file</i>	
Preparation/	
Sensitivity Codes	
Normal and/or	
Dist. Special	
A	

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE(When Data Entered)

## ABSTRACT

AlGaAs/GaAs heterojunction gate GaAs FETs have been fabricated with molecular beam epitaxy (MBE) and organometallic vapor phase epitaxy (OM-VPE), which allow for enhanced uniformity and reproducibility. The best results were obtained with MBE n-GaAs active layers and OM-VPE gate layers of  $p^+$ -AlGaAs and  $p^+$ -GaAs. Process steps such as a plasma ash and in situ heat cleaning of the mesa-etched layer before OM-VPE gate growth must be taken in order to ensure that the interface is clean and free of carbon contamination. Moreover, a very thin (200 Å)  $p^+$ -GaAs layer between the n-GaAs channel and the  $p^+$ -AlGaAs helps to isolate the actual  $p^+n$  gate junction from oxygen that is gettered into AlGaAs grown by OM-VPE. C-V measurements indicate a 1.3V built-in voltage for this junction, while forward I-V characteristics give a nonideality factor  $n = 2$  and are similar to those of a GaAs  $p^+n$  junction. Thus the electrical characteristics of the heterojunction are retained, along with the advantages of selective undercut etching and self-aligned metal.

Since normally-off HJFETs are desired for direct coupling of logic circuits, control of threshold voltage is very important. Although HJFETs with record high saturation currents were produced with buffered active layers grown by both chloride transport VPE and MBE, extremely good threshold voltage control (variations of 0.1-0.2V over a 1-cm<sup>2</sup> wafer) was achieved with MBE. Saturation currents for normally-off HJFETs followed a square law and were the highest on record, greater than 50  $\mu A/\mu m \cdot V^2$  for 3 x 300  $\mu m$  and 1 x 300  $\mu m$  gate devices. Pt-Au gate metal is especially useful for achieving self-aligned, undercut-etched 1- $\mu m$  gate devices with low gate resistance. Results are discussed in the light of various process alternatives for GaAs digital ICs, and possible future developments for the HJFET are outlined.

#### ACKNOWLEDGEMENT

This work was performed under the direction of R. L. Bell at the Solid State Laboratory of Varian Associates, Inc., Palo Alto, California, and was supported by the Naval Research Laboratory, Washington, D.C. Participants at Varian were, in alphabetical order:

Steve Bandy  
C. Burleigh Cooper III  
Shogo Hikido  
Timothy Maloney  
Ram Saxena  
Robert Tong

Help and encouragement of Drs. J. E. Davey and K. J. Sleger of NRL are gratefully acknowledged.

TABLE OF CONTENTS

<u>Section</u>	<u>Page</u>
1. INTRODUCTION . . . . .	1
2. EXPERIMENTAL INVESTIGATION . . . . .	6
2.1 HJFET Fabrication . . . . .	6
2.1.1 Overall Process . . . . .	6
2.1.2 Wafer Preparation for Heterojunction Growth	10
2.1.3 Gate Etch . . . . .	12
2.1.4 Anti-Leakage Cleanup Etches . . . . .	15
2.1.5 AuGe and PtAu Metal Gate Masks . . . . .	17
2.2 p-n Junctions . . . . .	18
2.3 HJFET Results . . . . .	20
2.3.1 3- $\mu$ m HJFETs with VPE Active Layers . . . . .	20
2.3.2 3- $\mu$ m HJFETs with MBE Active Layers . . . . .	23
2.3.3 OM and Ion-Implanted Active Layers . . . . .	26
2.3.4 1- $\mu$ m Pt-Au Gate HJFETs . . . . .	26
2.3.5 RF Tests . . . . .	28
2.3.6 Ring Oscillators . . . . .	35
3. DISCUSSION AND CONCLUSIONS . . . . .	41
4. REFERENCES . . . . .	46
5. DISTRIBUTION LIST . . . . .	48

## 1. INTRODUCTION

The first efforts to fabricate p-Al<sub>0.5</sub>Ga<sub>0.5</sub>As/n-GaAs heterojunction gate field-effect transistors (HJFETs)<sup>1,2</sup> used chloride-transport vapor-phase epitaxial (VPE) n-GaAs active layers and liquid-phase epitaxial (LPE) gate layers. An adequate p-n heterojunction was achieved, probably because of the slight meltback of the n-GaAs active layer during LPE. However, there were some problems with uniformity and minimum thickness of the LPE gate layers, as well as threshold voltage control problems with the VPE active layers, that would have to be corrected before the technique could be used to make integrated circuits.

In the next phase of the program at Varian,<sup>3</sup> the gate layers were grown by organometallic vapor-phase epitaxy (OM-VPE), which produced very uniform, reproducible gate structures, a substantial improvement over LPE. Meanwhile, a slight problem with the substrate/active layer interface was cleared up by growing a buffer layer in the VPE step, and the pH 7.05 superoxol etch for GaAs (which requires careful pH monitoring and frequent replacement) was replaced by citric acid. The OM-VPE gate layers usually suffered from considerable oxygen content in the AlGaAs, a fact that was always suspected but not verified by secondary ion mass spectrometry (SIMS) until after that phase of the program was over. The oxygen problem, along with uncertainties concerning wafer preparation and growth of the gate layers by OM-VPE, led to unsatisfactory heterojunctions and HJFETs whose performance was inferior to that of previous VPE/LPE HJFETs.

This stage of the HJFET program began with an intense effort to improve the heterojunction interface. The structure shown in Fig. 1 was adopted for the gates -- the extra thin layer of p-GaAs is possible with OM-VPE and was inserted in order to isolate the p-n junction from the AlGaAs. The in-diffusion of Zn dopant also helps to move the junction away from the AlGaAs. A GaAs p-n homojunction has nearly the same

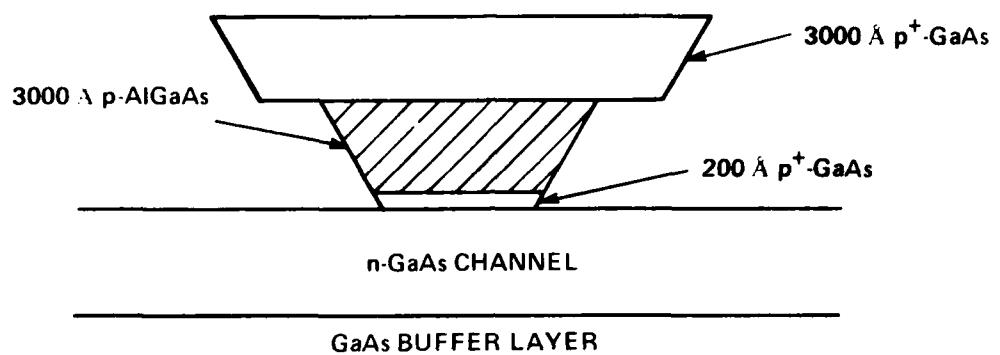


Fig. 1 Self-aligned JFET gate.

built-in voltage as an AlGaAs/GaAs heterojunction and should be similar to the ideal heterojunction as an FET gate. We will continue to refer to this device as an HJFET. AlGaAs is still needed, in order to retain the selective etching and self-alignment features of the device, but now the device is much less sensitive to oxygen contamination in the AlGaAs. We have at the same time developed gettering techniques to remove the oxygen from the AlGaAs, so the thin p-GaAs layer may not be required in the future.

Considerable attention was paid to preparation of the wafers before OM-VPE gate growth. For example, in order to avoid carbon contamination of the surface, photoresist residue must be removed by oxygen plasma ash and organic solvents must be avoided beyond a certain point. Details of these processes will be given in Section II. After much effort, the gate junctions were improved and HJFETs were performing well.

Figure 2 is a chart showing achievements in this program, when they came about, and approximate expenditures each month. The really major milestones are 1, 3, and 4 -- notice that each of these involved about the same expenditure. Milestone 2 (normally-off VPE/OM HJFETs) was achieved over part of a wafer when a VPE layer was thinned the proper amount. A really significant number of normally-off HJFETs had to wait for Milestone 3. This chart was prepared in order to summarize the results under this program, and to emphasize how much had to be expended just to get the HJFET working acceptably. It should be remembered that other achievements such as the characterization of various p-n heterojunction diodes and work on ring oscillator circuits (both discussed later) are not included in Fig. 2.

Nearly all the HJFETs reported in this work were fabricated with VPE and molecular beam epitaxy (MBE) for the n-GaAs active layers, and OM-VPE or MBE or the gate layers. MBE was most satisfactory for the

### MILESTONES

1	-	N-On VPE/OM	3- <sub>1</sub> - <sup>1</sup> m FET
2	-	N-Off VPE/OM	3- <sub>1</sub> - <sup>1</sup> m FET
3	-	N-Off MBE/OM	3- <sub>1</sub> - <sup>1</sup> m FET
4	-	MBE/OM Pt-Au	1- <sub>1</sub> - <sup>1</sup> m FET

### APPROXIMATE MILESTONE COST

1	-	\$24K
2	-	\$13K
3	-	\$29K
4	-	\$28K

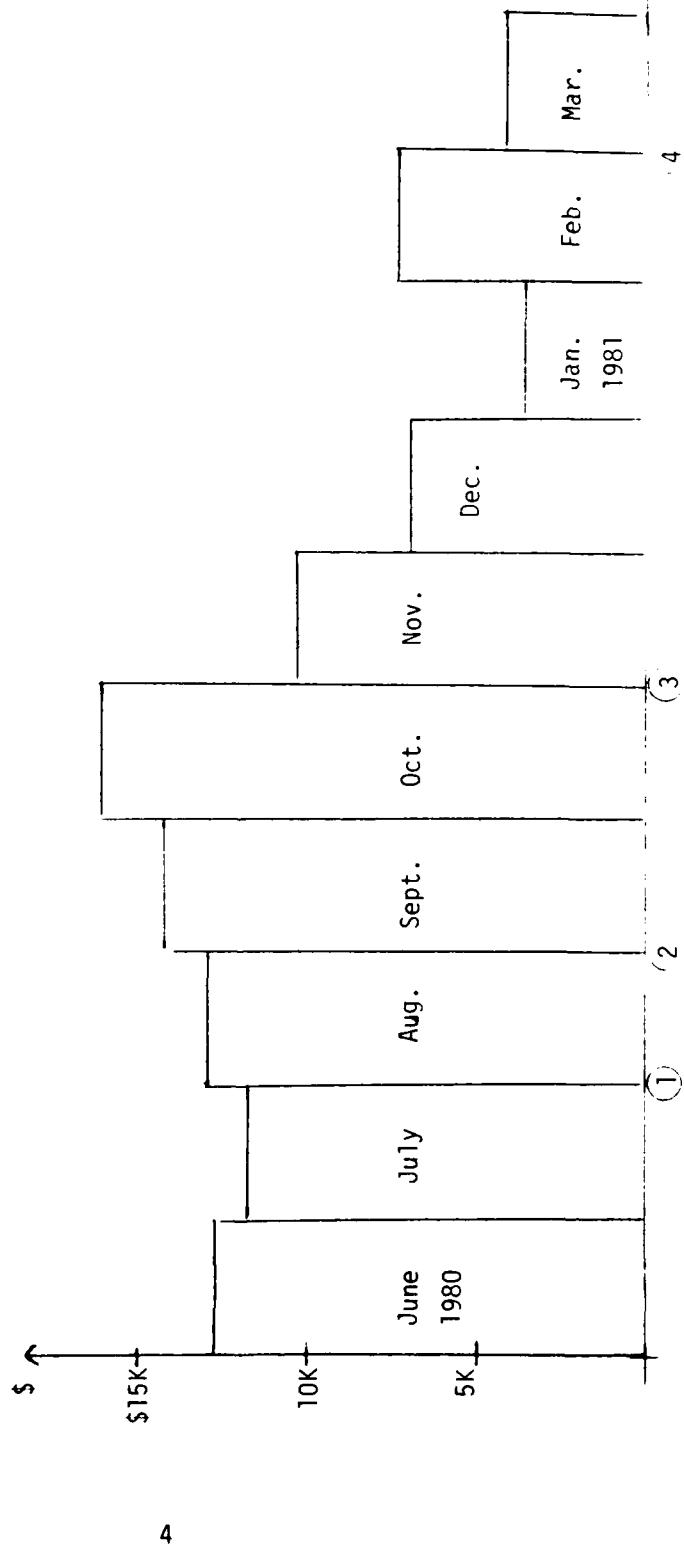


Fig. 2 HJFET achievements and spending.

active layer of normally-off (N-Off) HJFETs because very uniform thin layers could be grown. The best HJFETs resulted when these layers were mesa-etched and gates were grown by OM-VPE. MBE gates were tried, too, but performance was not good because in situ etch techniques before gate growth were not available with MBE as they were with OM.

## 2. EXPERIMENTAL INVESTIGATION

### 2.1 HJFET Fabrication

#### 2.1.1 Overall Process

The basic HJFET investigated has its heterojunction near a growth interface and is the same as reported previously,<sup>1-3</sup> a FET with two 150- $\mu\text{m}$  long gate stripes (Fig. 3). Connections are made to a gate pad, drain pad, and two source pads. Gate widths of 2, 5 and 7  $\mu\text{m}$  are available on alternate masks and the final width of the gate junction is determined by the undercut etch. In this work, the 5- $\mu\text{m}$  mask was used to simplify process development in the early stages, and later the 2- $\mu\text{m}$  mask was used. The resulting undercut gates were about 3  $\mu\text{m}$  and 1  $\mu\text{m}$ , respectively, and will often be referred to as such in this work. The basic process, emphasizing the alternatives available at two steps, is outlined in Fig. 4. Figure 5 is a more complete outline and focuses on the VPE and MBE active layers and OM gates, with which our most successful results were obtained. Comments on other process alternatives appear later.

An n-GaAs active layer doped at about  $10^{17}/\text{cm}^3$  is prepared by VPE or MBE, then mesa etched for isolation, and for low gate pad capacitance. Before FET processing, a VPE layer is grown thick (8-10V pinchoff with Au dots) and then is thinned appropriately. Normally-off devices were achieved when the pinchoff voltage at this stage was about 2V. This layer thickness requirement is due in part to the *in situ* HCl etch before OM gate growth, but is believed to be mostly due to the in-diffusion of the Zn dopant during OM gate growth. More about wafer preparation is discussed in the next section. The MBE layers can be grown to the proper thickness in one step and were usually not C-V characterized. The most successful MBE layers were doped at  $10^{17}/\text{cm}^3$  and nominally 1900  $\text{\AA}$  thick.

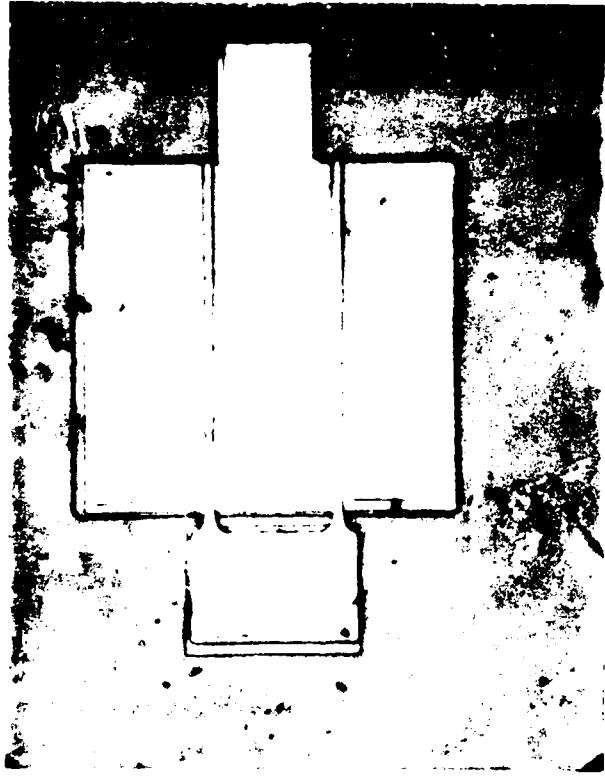


Fig. 3 Top view of completed HJFET.

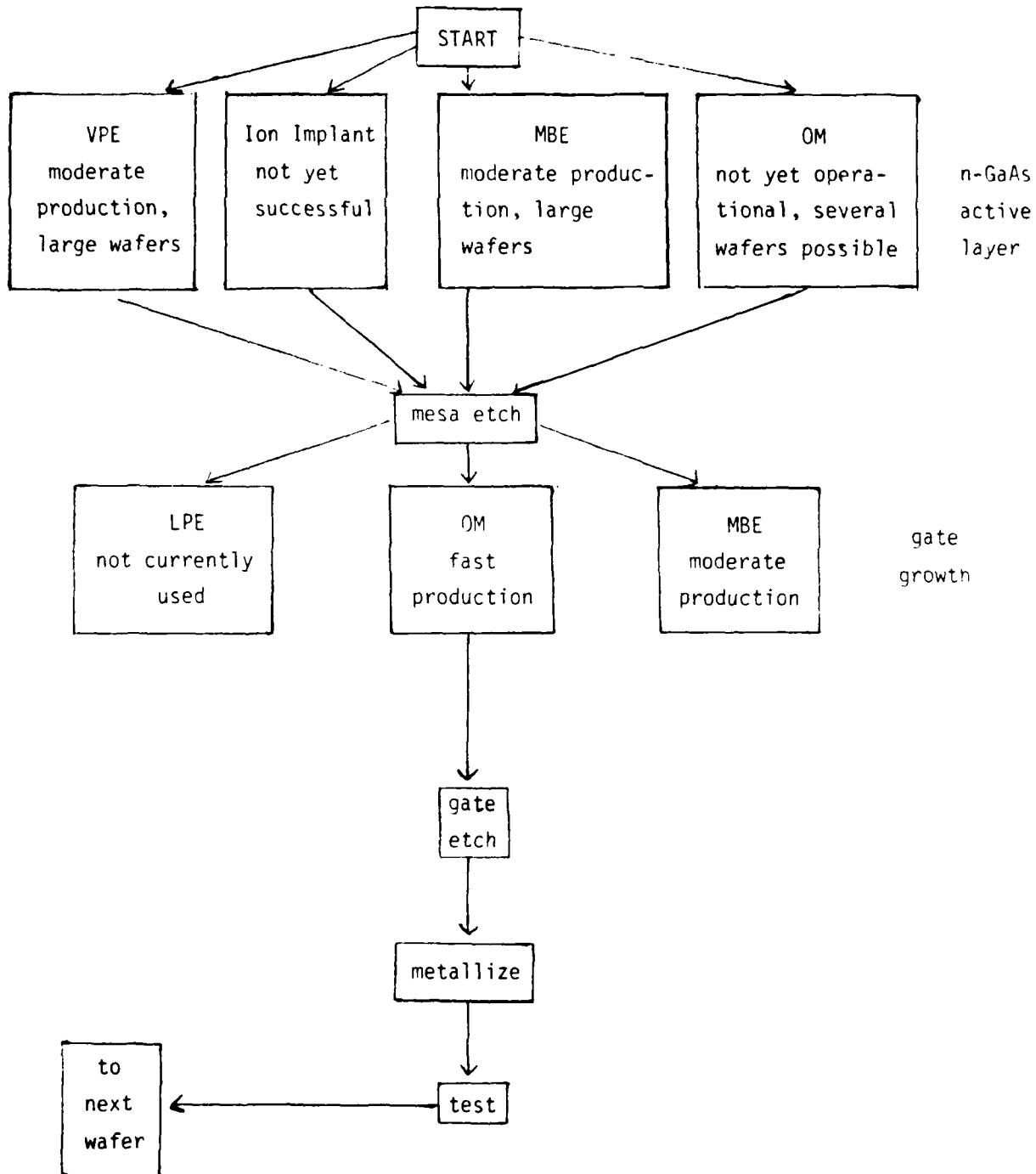


Fig. 4 Growth interface heterojunction FET process.

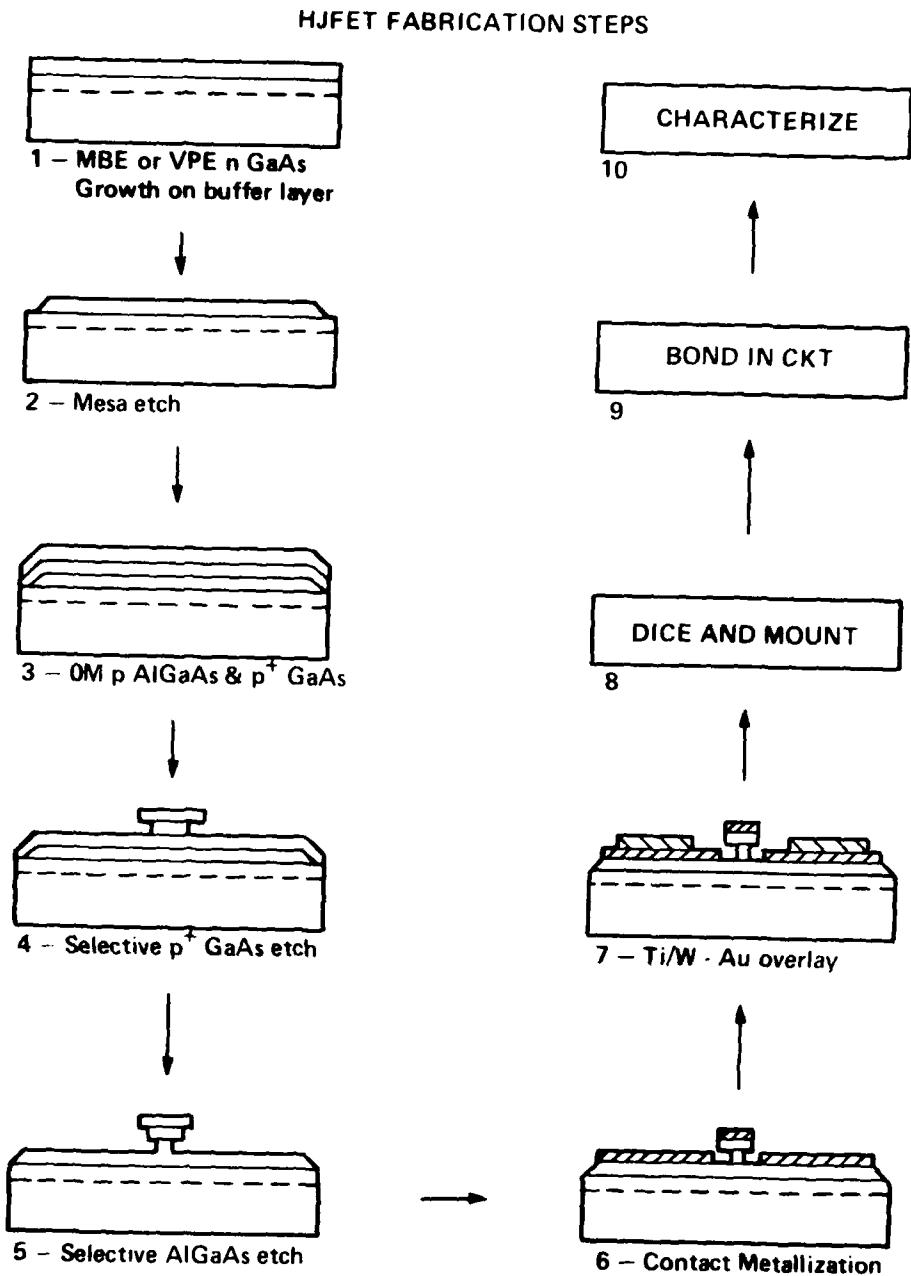


Fig. 5 Fabrication of heterojunction FET with OM gate layers.

After the mesa etch, the gates are grown by OM; then the gate mask is applied. Photoresist versus metal gate masks are discussed in Sec. 2.1.5. Selective etching with citric acid solution<sup>4</sup> and HF (discussed later) is done on the GaAs and AlGaAs, respectively. Ideally, a V-type gate cross section will result, as illustrated in Fig. 6. The semiconductor gate layers are thick enough to allow self-alignment of the AuGe/Ni/Au metal, applied in the next process step. The metal is alloyed at 450°C for 15 sec and results in a low-resistance ohmic contact to the source and drain. The devices can then be tested on a curve tracer. If desired, they can be readied for bonding by sputtering a metal overlay (1200 Å Ti-W/2000 Å Au), thinning to 150 µm, plating the backside with electroless Pd, and dicing. Chips are screened by visual and I-V checks, and are then die bonded and wire bonded into carriers suitable for common source microwave measurements on an HP automatic network analyzer system.

### 2.1.2 Wafer Preparation for Heterojunction Growth

The first attempts to use OM gates for HJFETs were hampered by oxygen-doped AlGaAs and by contamination due to processing before the gate growth.<sup>3</sup> Even when it was arranged to grow a heterojunction in the OM reactor, the oxygen at the interface severely degraded the performance. The present HJFETs were begun by adopting the thin p<sup>+</sup>-GaAs layer between the channel and the AlGaAs (as discussed earlier), to isolate the gate junction from oxygen. It was believed that wafer preparation for the OM gate growth was critical to obtaining a good junction, especially when such process refinements began to produce improvements in the HJFETs. A variety of procedures were permanently adopted for the mesa etch and wafer prep steps when high-performance FETs were finally achieved. These procedures are known to be sufficient, and most are believed necessary, although there was no strong motivation to study the latter exhaustively.

	AuGe/Ni/Au
	n - GaAs
	n = GaAs buffer
	p - Al <sub>0.5</sub> Ga <sub>0.5</sub> As
	p <sup>+</sup> - GaAs

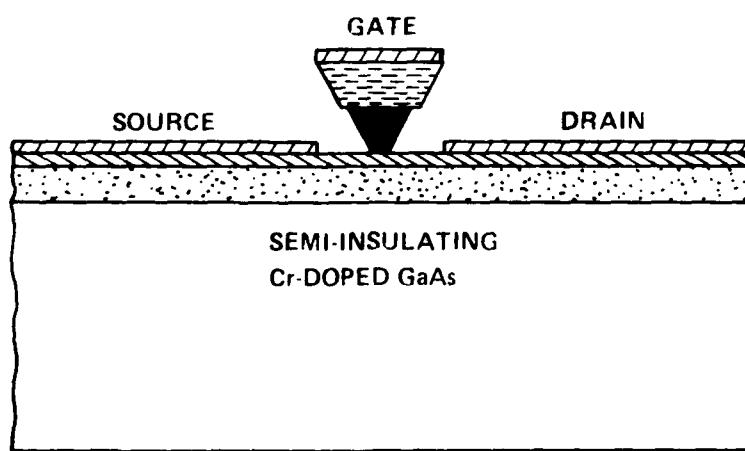


Fig. 6 Schematic Diagram of HJFET.

Since the VPE layers had to be thinned down and C-V profiled with Au dots at each step, some concern arose over how the Au would effect the GaAs surface, despite the fact that the dots were quickly removed. The heat of condensation of Au is known to be large enough to cause point defects in GaAs<sup>5</sup> and it is well known that Au dots will leave visible damage on a GaAs wafer if left on for, say, several weeks. In order to avoid a possible interfacial problem because of the Au dots, a sparse dot shadow mask was prepared so that very few of the resulting HJFETs will have had Au near the junction. The sparse dot mask is still quite adequate for C-V profiling and is now often used for production VPE MESFET material because of the concern over Au dot damage.

During the mesa etch step, there is photoresist on the very areas where the heterojunction will be. Since acetone does not completely remove AZ 1350J photoresist, there is a strong possibility of contamination from that hydrocarbon residue. In order to minimize this contamination, the wafer was oxidized in hot H<sub>2</sub>O before the mesa photoresist was deposited, so that after mesa etching some of the photoresist scum could be "lifted off" with HF. After that liftoff, the wafer was O<sub>2</sub> plasma ashed, to remove the rest of the scum, and a dilute HF solution removed the thin oxide formed during the plasma ash. No organic solvents were used after photoresist removal, to prevent carbon contamination. Immediately before loading into the OM reactor, the wafer was rinsed in straight H<sub>2</sub>SO<sub>4</sub>. Before the beginning of OM gate growth, there was a high-temperature cleaning step and a brief HCl etch, in order to clean off native oxides and slightly etch the wafer.

### 2.1.3 Gate Etch

The gate etch was done by well-known selective etch techniques. A citric acid/H<sub>2</sub>O<sub>2</sub> solution<sup>4</sup> with k = 10 was used to etch the GaAs and stop at the AlGaAs. Then HF (straight from the bottle or 1:1

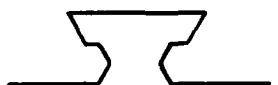
$H_2O:HF$ ) was used to etch the AlGaAs without etching the GaAs, so that an undercut was achieved. HCl also etches AlGaAs (especially when hot), but it was not used much in this work. It was found that the AlGaAs must be at least 50-60% Al in order to resist the citric acid etch, while for a pH ~.05 superoxol etch,<sup>1,2</sup> only 40-50% Al in the AlGaAs is required. The microprobe analysis used to estimate these percentages was done on ordinary HJFET wafers with 3000 Å thick AlGaAs layers. This was not quite thick enough for the depth of the microprobe electron beam, and the Al percentages could be known more accurately if special growth runs were done.

The cross section of the GaAs/AlGaAs selective etch is of some concern because the gate length, mechanical stability, and ability to evaporate self-aligned metal all depend on the gate etch. Self-alignment can be achieved as long as the AlGaAs is thick enough and there is some undercutting of the AlGaAs. For a short gate length, a V-type trapezoidal cross section is best, but is is difficult to arrange for this every time. Figure 7 shows gate cross sections that result when the gates are aligned parallel or perpendicular to elongated etch pits formed with 3:1:15  $NH_4OH:H_2O_2:H_2O$ . These etch pits distinguish the (110) from the (110) crystal directions.<sup>2-4</sup> Although the GaAs layer etches in the same way for each orientation, the AlGaAs layer may assume one of three shapes: V-trapezoid, inverted V-trapezoid, or hourglass. The alternatives shown in Fig. 7 are accompanied by numbers indicating how many times each was observed in the course of this work. Some of these cross sections seemed to correlate with whether or not the HF was diluted with water, with the percentage of Al in the AlGaAs, and with whether photoresist or metal was used as an etch mask, but no firm conclusions could be drawn. Eventually, the parallel direction was always used because a V-type AlGaAs cross section usually resulted. For narrow (2-μm mask) gates, the undercut for perpendicular orientation would usually separate the AlGaAs from the GaAs by the time the AlGaAs

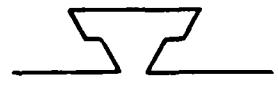
$\perp$  TO ETCH PITS:



(18)



(3)



(2)

$\parallel$  TO ETCH PITS:



(21)



(15)



(3)

Fig. 7 Citric acid/HF gate etch profiles.

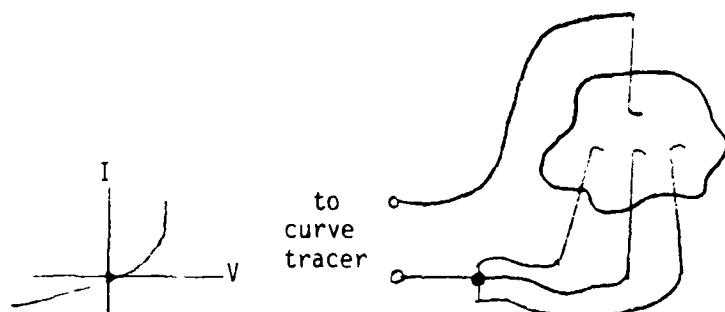
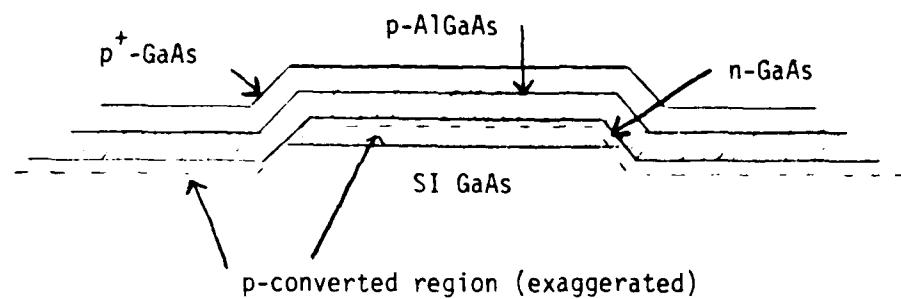
in the field was gone, and so for narrow gates the perpendicular direction could not be used at all. The GaAs/AlGaAs etching is manageable but is a good deal more complicated than previously reported.

Sometimes, following the HF etch of AlGaAs, the gate fields would have patches of AlGaAs which would either not etch off or would etch off only after prolonged immersion in HF. The latter alternative would destroy the FET gates and was not acceptable. The effect may have been due to a slight grading in the Al percentage near the interface, evidence for which is provided by the occasional success of 3:1:90 ( $\text{NH}_4\text{OH}$ : $\text{H}_2\text{O}_2$ : $\text{H}_2\text{O}$ ) in removing the AlGaAs patches. This etch removes both GaAs and AlGaAs. However, the best way to avoid these interfacial problems was to move the wafer into the HF etch directly from the water bath used to stop the citric acid etch. The wafer should not be dried between etches.

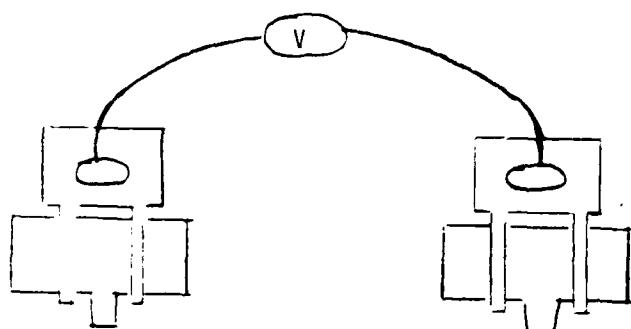
#### 2.1.4 Anti-Leakage Cleanup Etches

Following the citric acid and HF gate etches, there is still a thin layer (a few hundred angstroms) of p-GaAs on top of the n-GaAs channel, due to the in-diffusion of Zn and to the growth of a thin p-GaAs layer below the AlGaAs. In the semi-insulating mesa field, the p-converted layer due to Zn diffusion is expected to be thicker because the background doping is much lower. This means that removal of the p-layer has to be done in two steps. The p-layer is first completely removed from the mesa with a brief citric acid etch (usually 5-10 sec for a  $k = 10$  etch). If wax is used to include a large mesa on the wafer at the time of the mesa etch, the material can be monitored for a change from p to n, as shown in Fig. 8. Three point contacts are shorted and applied with heavy pressure to approximate an ohmic contact, while one point contact is applied lightly to approximate a rectifying contact.

This technique was not completely reliable because it was difficult to



Point probe test of large  
mesa (n-GaAs) during  
etchback



Check of device-to-device isolation during  
etch of mesa field only

Fig. 8 Leakage current due to Zn diffusion.

establish the proper ohmic and rectifying contacts with the point probes, but it could probably be improved by wetting a probe with a liquid metal (Hg or Ga-Sn) for the rectifying contact. When Pt-Au metal gates were used for the gate etch, it was possible to monitor gate-to-epilayer leakage on the large mesa with the point probes until a leak-free n-type characteristic was achieved.

The rest of the p-converted layer in the mesa field must also be etched off so that it does not provide leakage paths between source, gate, and drain pads. It is best to complete the AuGe contact processing before attempting this etch, in order to avoid breaking the gates at the mesa edge. The FET channel may now be protected with the mesa mask, or with the (clear field) metal mask double exposed with the (dark field) overlay mask. The mesa mask allows monitoring of this etch by checking device-to-device isolation (see Fig. 8) while the double exposure scheme allows that as well as the complete I-V characterization of a device during etchback. Ten to twenty seconds of citric acid etch are typically required. Dramatic improvements in gate leakage were often seen with this etch.

#### 2.1.5 AuGe and PtAu Metal Gate Masks

The AuGe/Ni/Au self-aligned metal is chosen for low contact resistance on the source and drain (about  $10^{-6}$  ohm-cm<sup>2</sup>). If photoresist is used for the gate etch, then the same metal contacts the p-type GaAs gate but with a contact resistance of about  $10^{-4}$  ohm-cm<sup>2</sup>.<sup>1</sup> If a metal chosen to give low contact resistance to p<sup>+</sup>-GaAs could also be used as a gate etch mask, low contact resistance would be achieved for all connections. In the past, this failed in the case of Au-Mg and superoxol etching of GaAs because of uneven undercutting.<sup>1</sup>

Our first attempts at etching with citric acid/HF and a metal mask were with AuGe/Ni/Au metal, since it is easy to include an extra wafer

in an ordinary evaporation. The results after etching were variable, but in some cases the etch profile was quite acceptable. Some irregularities, including frequent pitting of the metal during the etch, discouraged further work on AuGe. When it was reported that Pt-Au (1000-2000 Å, respectively) was an acceptable gate mask as well as a low resistance contact to GaAs,<sup>6</sup> it was tried and used with considerable success. Some procedures described in Ref. 6 had to be modified. The 3-minute alloy of the Pt-Au had to be done before the AuGe evaporation and after the gate etch. If the Pt-Au alloy precedes the gate etch, the gate metal peels off from many gates if any citric acid etching follows. This indicates a very shallow alloy of the Pt-Au, which may be useful. After the AuGe/Ni/Au self-aligned metal was evaporated, the usual 15-sec, 450°C alloy was done. Figure 9 shows an example of a gate etch profile using Pt-Au as a mask. Pt-Au also lowered the gate resistance of the HJFETs, as will be shown later.

## 2.2 p-n Junctions

The principal aim of this HJFET technology is normally-off FETs for logic circuits. The built-in voltage of the heterojunction is larger than that of a metal Schottky contact, meaning that a larger voltage swing results and thicker epitaxial layers can be used. The p-n junction must live up to expectations, however, in order to achieve these goals. We therefore began to observe I-V and C-V characteristics of 20-mil dot heterojunctions once good FETs were achieved.

With the N-Off HJFETs, the forward gate current invariably reaches the same scale as the ( $V_g = 0$  to +1V) source-drain saturation current at +1-1.2V on the gate, as will be shown later. This is not as high as one would expect if the heterojunction behaved like a Schottky barrier with a built-in voltage of about 1.4V, nor was such an I-V characteristic observed with the 20-mil heterojunction dots. Despite one claim that the p-AlGaAs/n-GaAs heterojunction behaves like a Schottky barrier with

Pt/Au Metal Mask Expt  
CM 965 13,160 X 3 min at  
⑧ Sum practice gates 8 sec HF  
12-5-80



Fig. 9 Gate etch using PtAu as a mask.

built-in voltage  $V_{bi} = 1.36V$  and a nonlinearity factor of 1.57,<sup>7</sup> most observers of AlGaAs/GaAs p-n heterojunctions (in addition to AlGaAs and GaAs p-n junctions) report much higher current density scaling constants and nonideality factors of about 2, both because of surface recombination.<sup>8-10</sup> Our forward I-V characteristics (Fig. 10 is typical) were in strong agreement with Refs. 8-10. Figure 10 is an I-V characteristic for a 20-mil dot growth interface heterojunction; i.e., processed in the same way as the FETs. Grown p-n junctions (both AlGaAs/GaAs and GaAs p-n homojunctions) had only slightly lower current densities. C-V characteristics for all of the grown junctions and most of the growth interface heterojunctions gave built-in voltages of 1.3-1.4V. Occasionally, the growth interface heterojunction would appear to have  $V_{bi} = 1-1.1V$ , probably because of interface states.<sup>11</sup> But if any of the I-V characteristics was subjected to the thermionic emission analysis of Ref. 7,  $V_{bi}$  would be 1 to 1.06V, clearly out of line with the more believable C-V results.

### 2.3 HJFET Results

#### 2.3.1 3- $\mu m$ HJFETs with VPE Active Layers

The first successful HJFETs having OM gate layers were fabricated with VPE n-GaAs active layers, used the 5- $\mu m$  gate mask, and had all connections metallized with AuGe/Ni/Au. The first HJFET with really satisfactory performance was normally-on, as intended, and I-V characteristics appear in Fig. 11. Saturation currents in this and other HJFETs approximately follow a square law:

$$I_{ds} = KZ(V_g - V_t)^2$$

where  $V_g$  is the gate voltage,  $V_t$  is the threshold voltage, Z the gate periphery, and K is a scaling constant. The scaling constant, K, is therefore

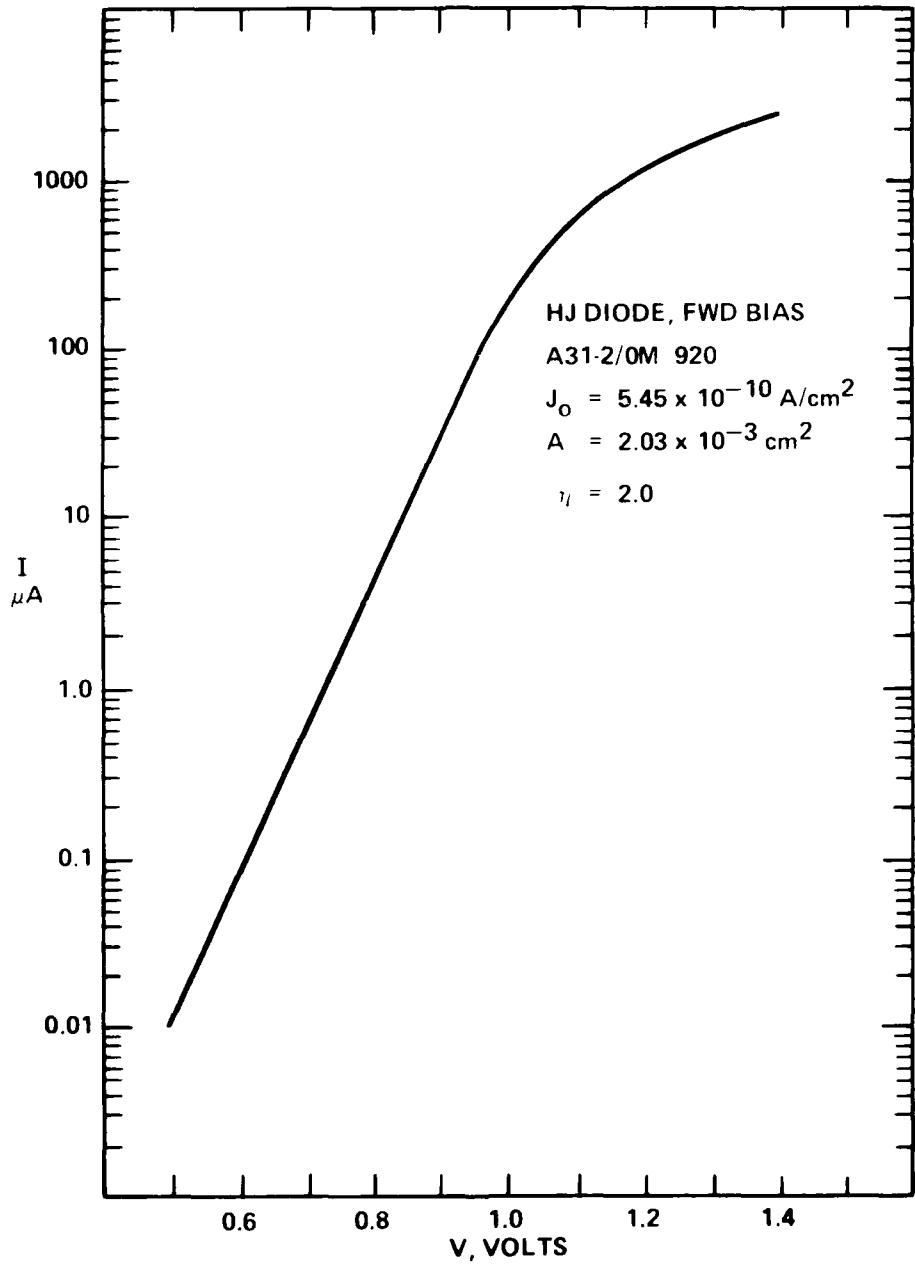
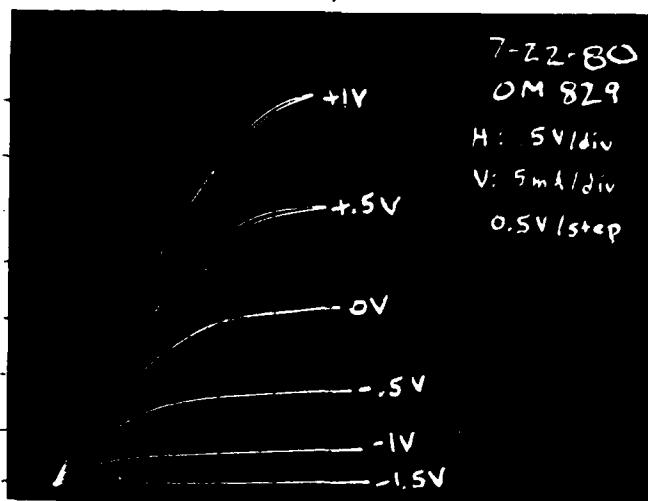
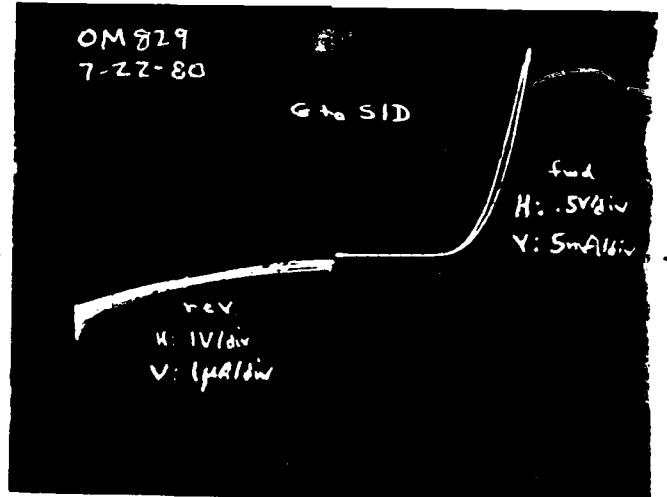


Fig. 10 I-V for 20-mil HJ diode on A31-2/OM 920.



a) FET I-V characteristic.

$K = 35$



b) Gate to source/drain.

Fig. 11 VPE/OM N-On HJFET.

a measure of transistor performance and will, for simplicity, be used to compare FETs. The units of K given in the figures are  $\mu\text{A}/\mu\text{m-V}^2$ .

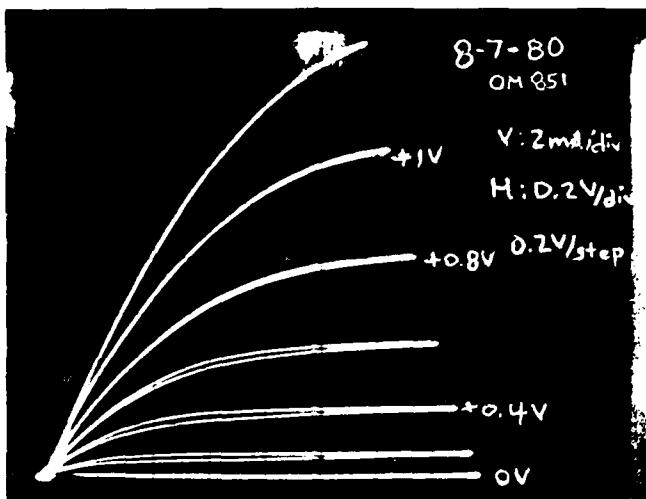
After appropriate thinning of a VPE layer and growth of OM gates, normally-off FETs resulted over part of the wafer.  $K = 40 \mu\text{A}/\mu\text{m-V}^2$  was achieved, and the I-V result is in Fig. 12.

MBE gate layers were tried once with a VPE active layer, but without significant results. The source-drain currents were reasonable ( $K = 33 \mu\text{A}/\mu\text{m-V}^2$ ), but the forward gate characteristic was impeded by a resistive layer. The unavailability of in situ etch techniques for the MBE gate growth may have been responsible for this difficulty. Al percentage in the AlGaAs was not easy to control for the MBE and so not much further work was done on MBE gates.

### 2.3.2 3- $\mu\text{m}$ HJFETs with MBE Active Layers

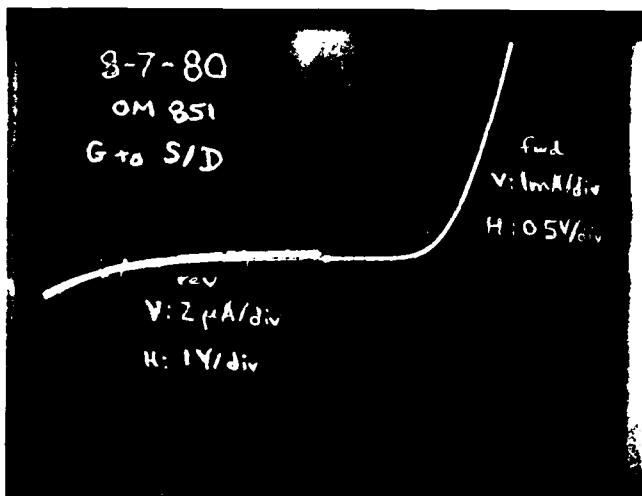
The first attempts to fabricate HJFETs having MBE active layers and OM gates resulted in very leaky devices because of surface defects in the MBE material. The MBE material soon improved, just as it was becoming clear that threshold voltage control was very difficult to do by thinning VPE layers. The normally-off MBE/OM HJFETs of Fig. 13, with  $K = 53 \mu\text{A}/\mu\text{m-V}^2$ , performed better than any previous HJFETs. In addition, the yield over two wafers (MBE 530 and MBE 537) was high, and the threshold voltage ranged from 0 to +0.2V, a tolerance made possible by the extreme uniformity of MBE.

MBE gates were tried once on a mesa etched MBE active layer but the resulting FETs were leaky because of the leakiness of the active layer material. When the OM gate process proved so successful, MBE gates were not attempted any further.



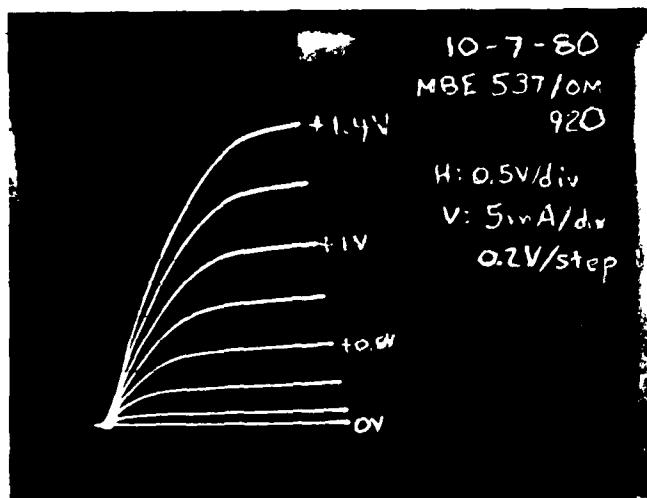
a) FET I-V characteristic.

$K = 40$



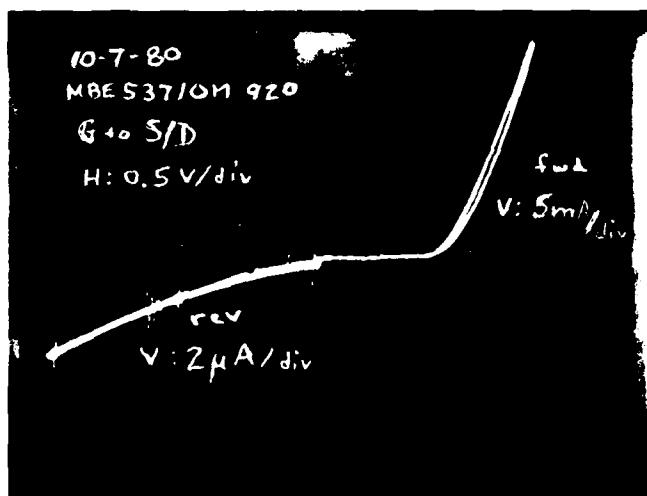
b) Gate to source/drain.

Fig. 12 VPE/OM N-Off HJFET.



a) FET I-V characteristic.

K = 53



b) Gate to source/drain.

Fig. 13 MBE 537/OM 920, HJFETs.

### 2.3.3 OM and Ion-Implanted Active Layers

The only process alternatives of Fig. 4 not discussed thus far are the use of ion implantation and OM for active layers. One ion-implanted layer (Si, 100 keV,  $2 \times 10^{12}/\text{cm}^2$ ), was run through the OM gate process and metallized, but the devices suffered from source/gate shorts. This may have been because a single-dose implant will have less dopant near the surface and thus can acquire a deeper p-converted layer because of Zn diffusion. A double implant, or a very accurate monitoring of the cleanup etch of the p-converted layer (Sec. 2.1.4), was felt to be necessary for ion-implanted active layers, and no further work on them was done.

At present, the biggest challenge facing OM epitaxy for FET active layers is the substrate-channel interface. Undoped buffer layers are likely to be more heavily doped than VPE or MBE buffer layers, and the difficulties of growing directly on Cr-doped substrates are well known. A few attempts were made (on another contract) at OM growth of Se-doped active layers on undoped substrates. One of these resulted in a 2-2.5V pinchoff,  $5 \times 10^{16}/\text{cm}^3$  layer, and so it was processed with the OM HJFET schedule using the 2- $\mu\text{m}$  gate mask. Figure 14 is the I-V characteristic of the resulting 1- $\mu\text{m}$  gate FETs. The large loops occurred with every device and indicate a problem with traps at the substrate-channel interface. Recently,  $\text{SiH}_4$  has been shown by the Varian OM Group to be a controllable n-type dopant gas, better than  $\text{H}_2\text{Se}$ .

### 2.3.4 1- $\mu\text{m}$ Pt-Au Gate HJFETs

The Pt-Au gate process, described earlier, was successfully used with the 2- $\mu\text{m}$  gate mask to fabricate narrow-gate HJFETs. The first successful run, MBE 609/OM 1036, was being processed as it was discovered that any narrow gates must be parallel to the etch pits (see

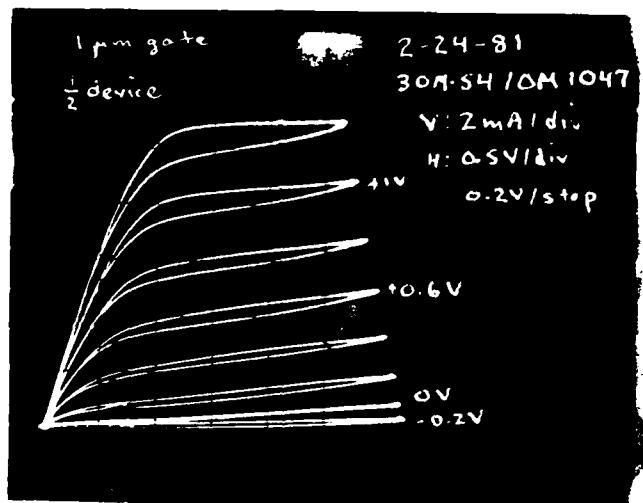


Fig. 14      $1 \times 150 \mu\text{m}$  gate HJFET made with  
 $5 \times 10^{16}/\text{cm}^3$  Se-doped OM active layer

Sec. 2.1.3), and so the run was saved from certain destruction by double exposing the gate mask in the parallel direction to give the device shown in Fig. 15. Because of the double exposure, the average gate width was about 1.5  $\mu\text{m}$ . Some good normally-on HJFETs resulted (Fig. 16), with low reverse leakage and low gate resistance. A later run of 1- $\mu\text{m}$  Pt-Au gate HJFETs (MBE 530/ OM 1091) gave similar low gate resistance but was more leaky (the MBE active layer was fogged) and  $K$  was lower, at 27  $\mu\text{A}/\mu\text{m} \cdot \text{V}^2$ .

Normally-on HJFETs with 7-8V pinchoff were fabricated with a VPE active layer and OM gates to give the results shown in Fig. 17. Despite slight  $g_m$  compression near  $V_g = 0$ ,  $I_{dss}$  (70 mA) is higher than that of a similar N-On device made by VPE/LPE,<sup>2</sup> and equal to that of a reported HJFET with 12V pinchoff.<sup>6</sup> Reverse gate leakage was so low (5 nA at -6V in one case) that it was difficult to photograph.

An illustration of the gate resistance improvement of Pt-Au over AuGe as a gate metal is shown in Fig. 18. Both FETs had 1- $\mu\text{m}$  gates and comparable source-drain characteristics, and the asymptotic behavior of the forward gate curve indicates an improvement in gate resistance of a factor of 3 or 4.

### 2.3.5 RF Tests

Two HJFETs were rf tested from 2-14 GHz on the automatic network analyzer, one N-Off FET with 3- $\mu\text{m}$  AuGe gates (MBE 537/OM 920), and one N-On FET with 1- $\mu\text{m}$  Pt-Au gates ( $V_t = -0.8\text{V}$ , MBE 609/OM 1036). The measured y-parameters were used in a simplified circuit model program and the source resistance was measured by dc methods to give the results in Figs. 19 and 20. The most striking result was the lower rf gate resistance measured for the Pt-Au gate. Although some variation with frequency was observed with this crude circuit model, the basic

MBE 609/OM 1036 HJFET 2-11-81  
⑪ 2 μm  
Pt-Au gates

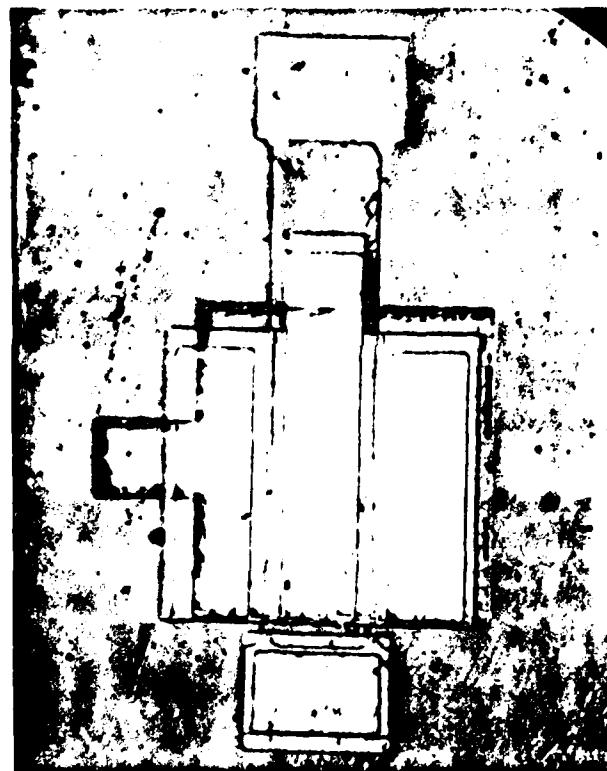
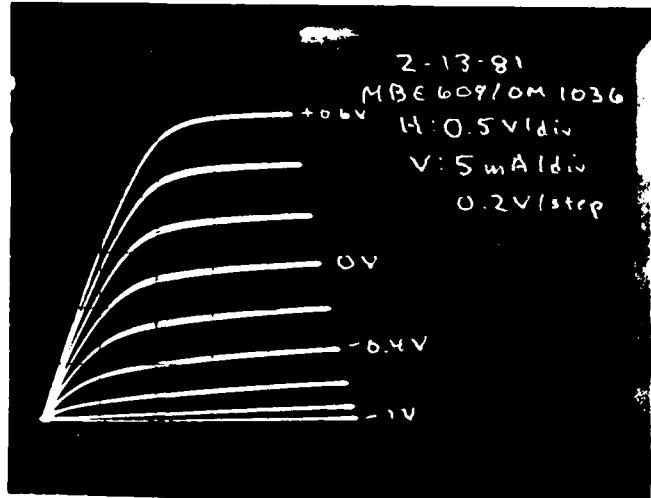
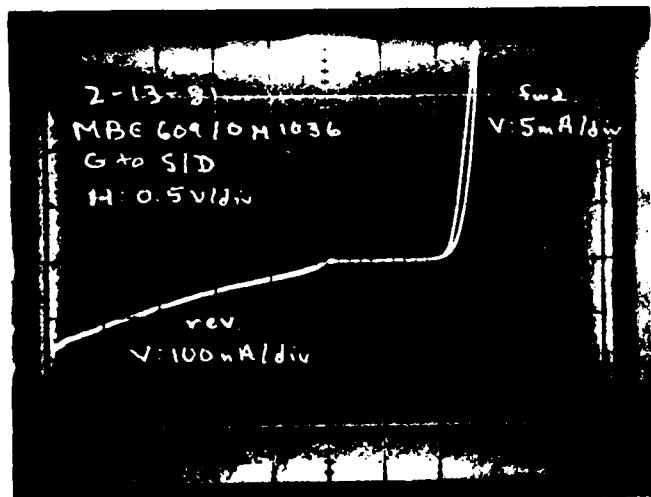


Fig. 15 Top view of MBE 609/OM 1036 HJFET with Pt-Au gates.



a) FET I-V characteristic.

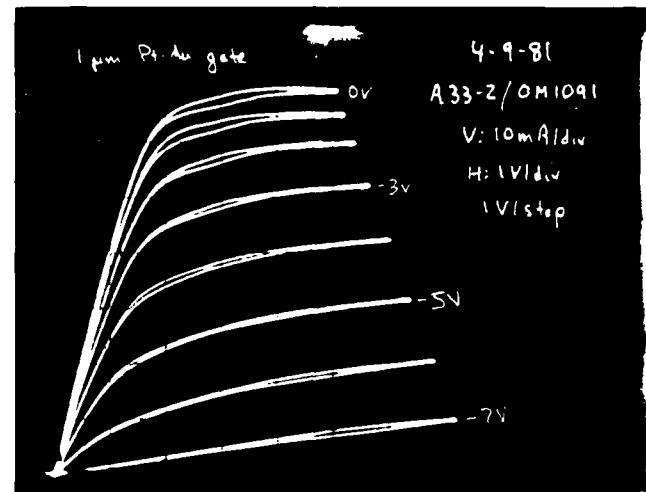
K = 55



b) Gate to source/drain.

Fig. 16 1-μm Pt-Au gate HJFET.

a) FET characteristic,  
 $V_t = -8V$



b) Gate to source/drain;  
forward voltage

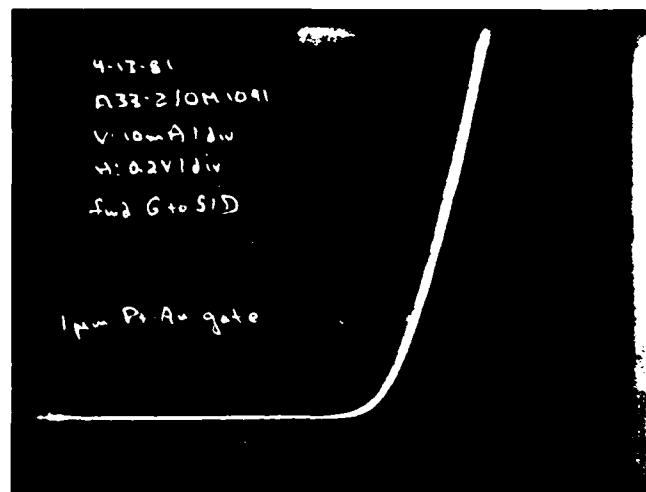


Fig. 17 VPE/OM N-On HJFET with 1-μm Pt-Au gates.

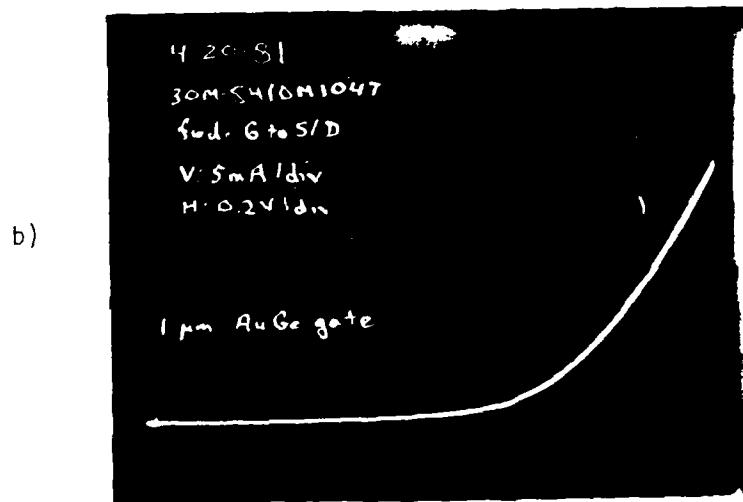
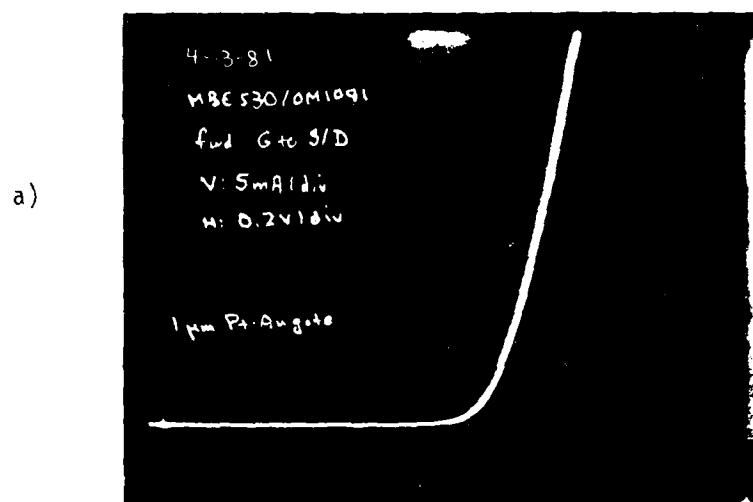
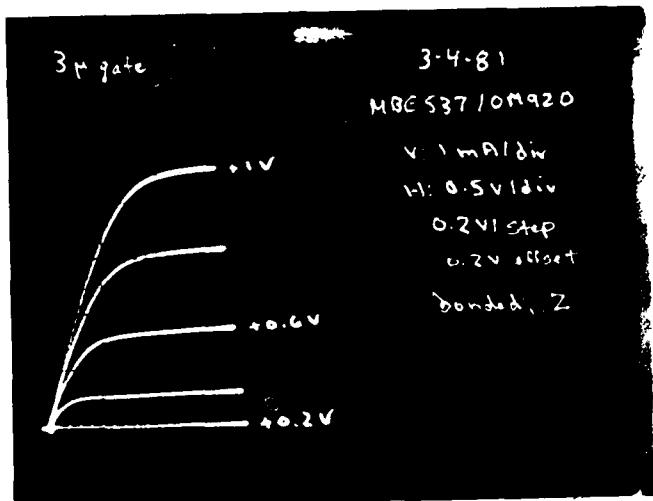


Fig. 18 Forward gate characteristic compared for  
a) Pt-Au and b) Au-Ge 1- $\mu$ m gates.

N-Off HJFET



Au-Ge/Ni/Au gate, 3  $\mu$ m

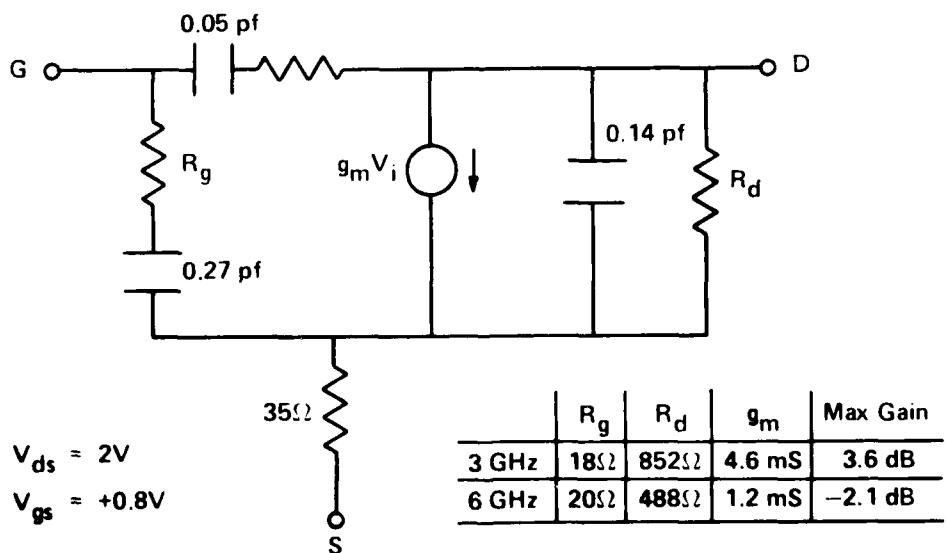
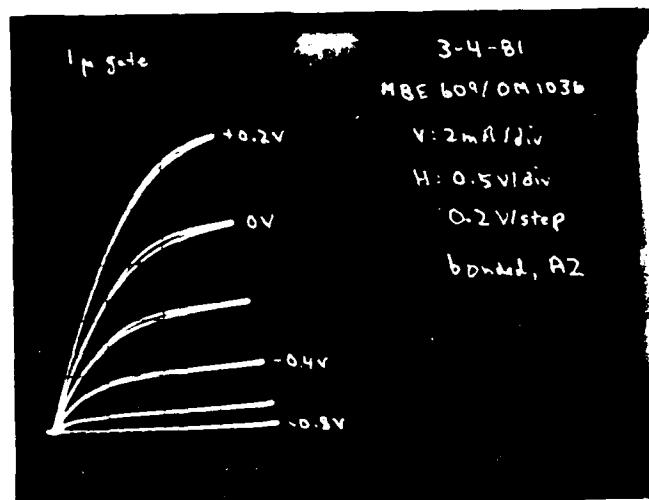


Fig. 19 RF characterization of MBE 537/0M 920 HJFET.

N-On HJFET



Pt-Au gate, 1  $\mu$ m

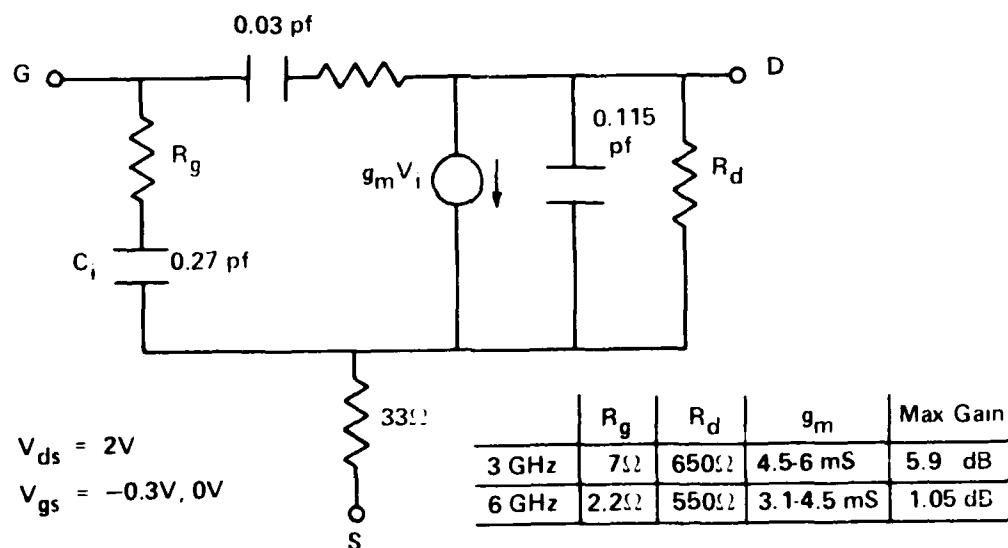


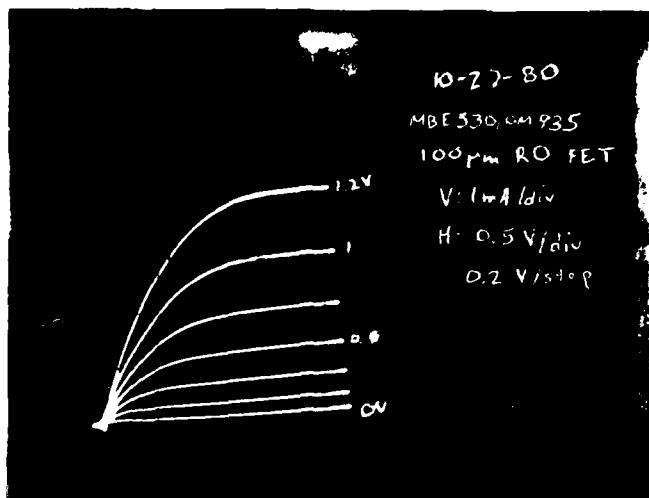
Fig. 20 RF characterization of MBE 609/OM 1036 HJFET.

gate resistance result is supported by the fact that  $g_{21}$  (the real part of the admittance parameter  $y_{21}$ , strongly dependent on the current source  $g_m v_i$ ) drops very steeply for the AuGe gates, but not for the Pt-Au gates.

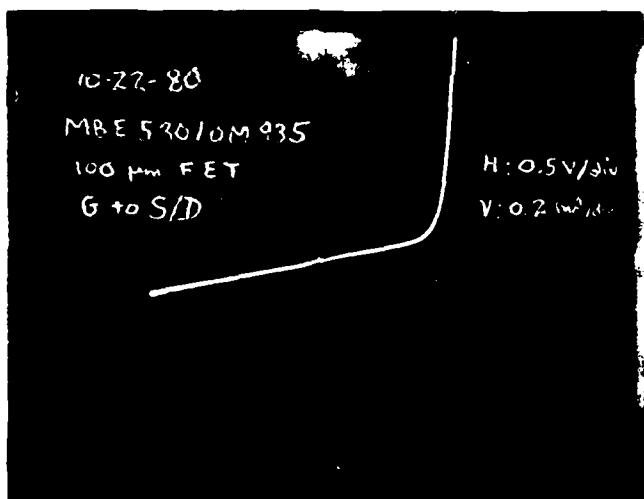
The FETs tested could have been better and, had budget constraints allowed, more rf tests would have been performed. Any further rf tests should be done on devices with low gate leakage currents as well as high saturation currents. The gate leakage current for the tested FETs was on the 100- $\mu$ A scale and may have interferred with the formation of a gate-drain space charge domain, leading to the unexpectedly high gate-drain feedback capacitance.

### 2.3.6 Ring Oscillators

The ring oscillator mask set, originally designed some years ago for MESFET ring oscillators (ROs), was used in several attempts to fabricate HJFET ROs and inverters. Reference 3 contains a description of the mask layout and the slight variations on the HJFET process that are used. Soon after the successful N-Off MBE 530/OM 920 HJFETs were fabricated, another piece of the same wafer was used with the RO mask set to give acceptable N-Off HJFETs with  $3 \times 100 \mu\text{m}$  gates, but with unexpectedly high gate leakage (Fig. 21). Figure 22 gives the inverter load's 2-terminal I-V characteristic and the rather poor voltage transfer characteristic. The photographs in Figs. 21 and 22 were prepared before some subtle points were recognized. When the mesa fields were etched as described in Sec. 2.1.4 to cut leakage, the much improved gate I-V and transfer characteristic of Fig. 23 resulted. But because the output voltage for zero input was nowhere near the supply voltage, the stability of the load I-V characteristic was suspected and the experiment indicated by Fig. 24 was done. Circuit ground gates the load I-V characteristic and causes a large voltage to be dropped across the load,



a) FET I-V characteristic.



b) Gate to source/drain.

Fig. 21 MBE 530/OM 935 Ring oscillator, 100 μm HJFET.

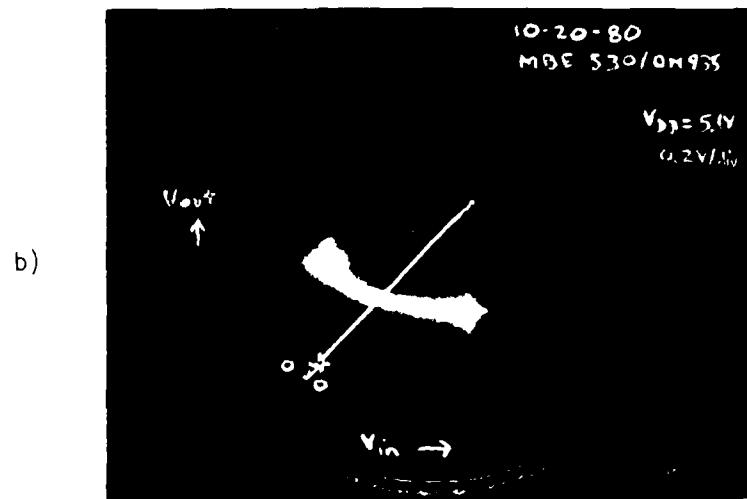
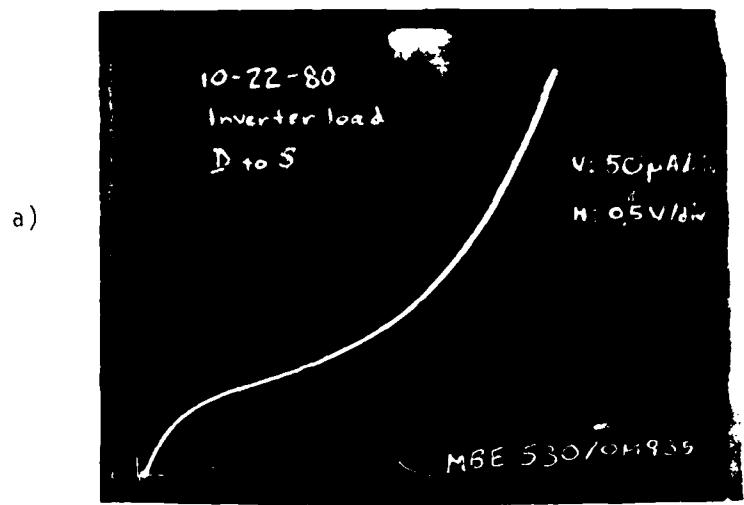
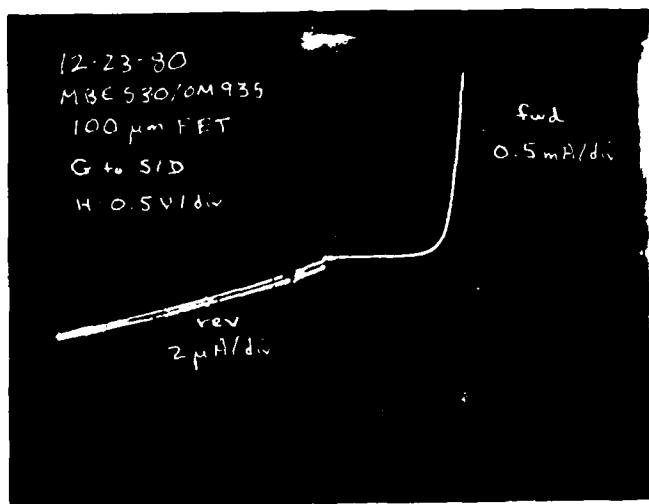
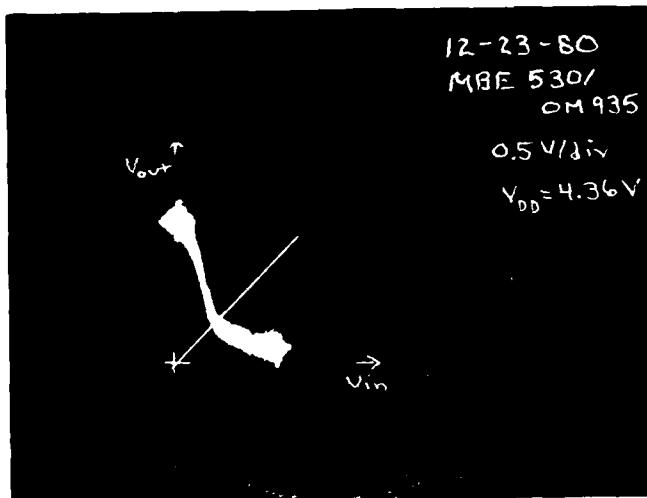


Fig. 22 MBE 530/OM 935 ring oscillator.  
a) inverter load and b) inverter transfer characteristic.



a) Gate to source/drain of FET.



b) Inverter transfer characteristic.

Fig. 23 MBE 530/OM 935 ring oscillator components,  
after antileakage etch.

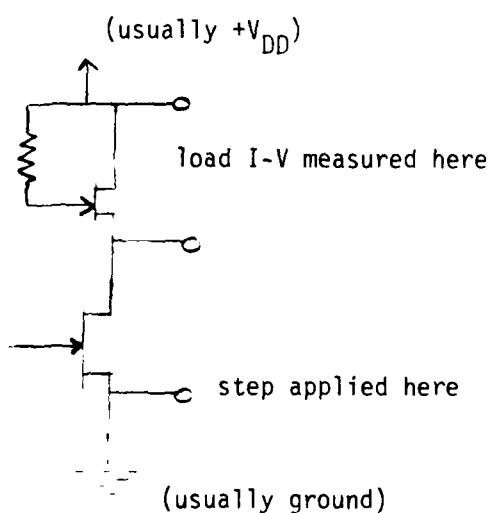
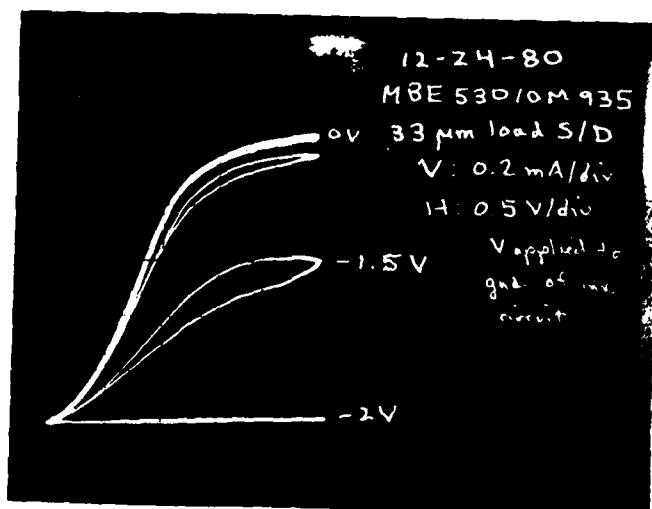


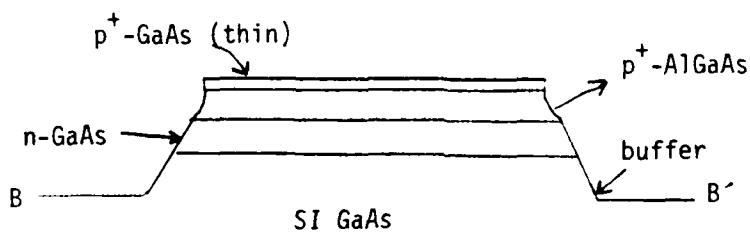
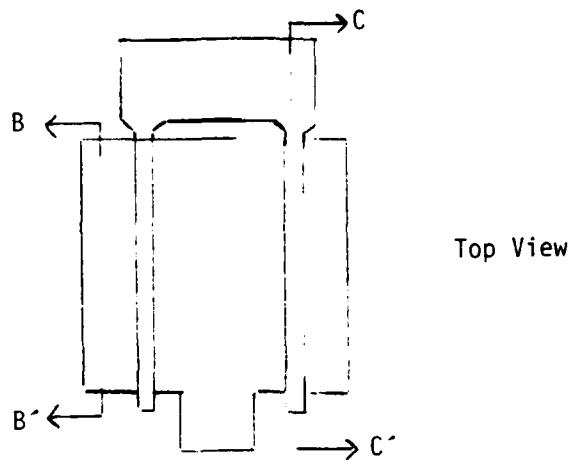
Fig. 24 Influence of circuit ground on inverter load.

even with no input voltage on the inverter, thereby degrading the voltage transfer characteristic. The reason for this is not well understood, but a few other measurements ascertained that the load's bias resistor was in the neighborhood of 100 K ohms, much higher than expected. Thus the load gate was almost floating, susceptible to low voltages nearby which could turn off the load transistor while drawing little current. We tried to remedy this decoupling of load gate and supply voltages by evaporating a small amount of metal on the bias resistor path. For this and one other R0 wafer, the attempt failed, only because of difficulties that arose with existing metal during the extra process step.

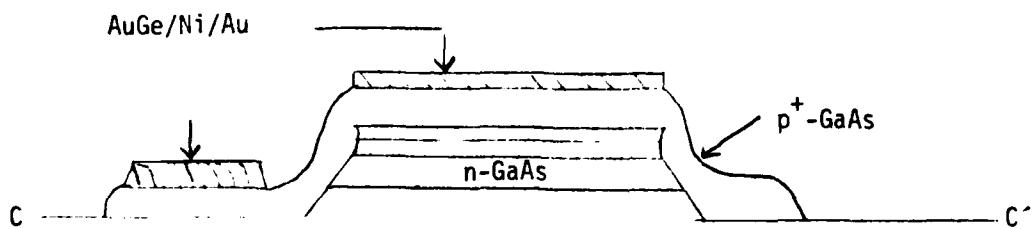
### 3. DISCUSSION AND CONCLUSIONS

It is clear from the foregoing results that the quality of AlGaAs/GaAs HJFETs has advanced considerably in this work. We have demonstrated  $1 \times 300$  and  $3 \times 300 \mu\text{m}$  normally-on and normally-off HJFETs with record saturation currents, and low gate resistance when Pt-Au is used on the gate. Moreover, the dc performance of these FETs measures up to that of  $1\text{-}\mu\text{m}$  gate ion-implanted GaAs JFETs made by e-beam lithography, also intended for digital IC applications.<sup>12</sup> The HJFET approach offers some advantages over e-beam lithography, since the devices are batch-processed with optical lithography and the  $1\text{-}\mu\text{m}$  (or submicron) gates are achieved with  $2\text{-}\mu\text{m}$  minimum linewidth masks. Also, sidewall capacitance of the gate junction should be lower with the HJFET than with the ion-implanted JFET. Superior rf performance is yet to be demonstrated with the HJFET, since only two unspectacular devices were characterized in this work; however, there is no reason to suspect a fundamental limitation.

The major technological difficulties now associated with the HJFET are reproducibility and yield of the devices. The MBE and OM epitaxial technologies give excellent uniformity of threshold voltage over a wafer, but reproducibility of threshold voltages from run to run is questionable, especially with the growth interface HJFET process. If the grown-junction scheme proposed in Fig. 25 works, it could solve the threshold voltage control problem as well as sidestep wafer preparation before gate growth. The crucial question is whether the final layer of  $p^+/\text{GaAs}$  will overgrow the mesa properly. The scheme could be tried at Varian now, but it was not really possible in the early part of this program. An MBE approach to step (a) would have had to wait for better AlGaAs, while an OM approach (growing on a VPE or MBE buffer layer) would have had to wait for the n-type dopant to be brought under control.



a) MBE growth of all layers, followed by mesa etch  
(before gate etch).



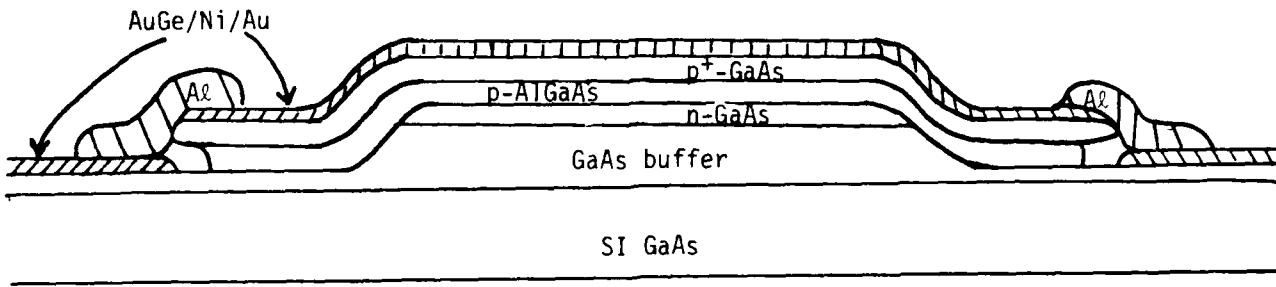
b) OM overgrowth of  $p^+$ -GaAs, followed by usual process.

Fig. 25 Proposed grown junction HJFET with mesa isolation.

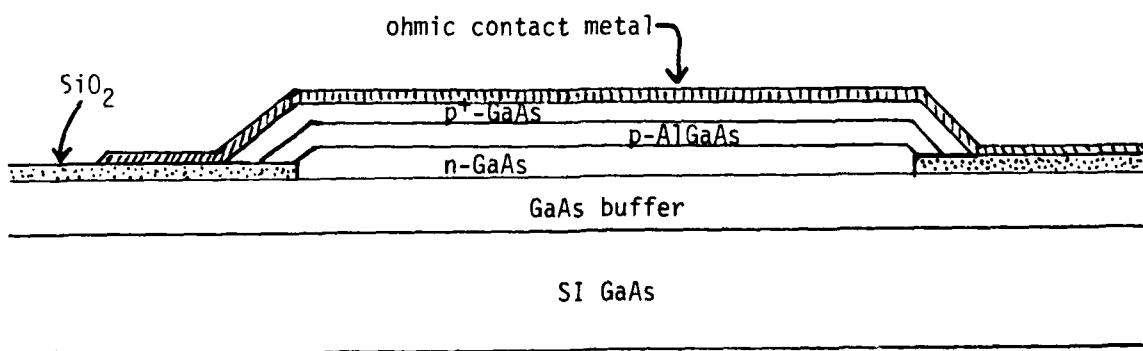
The use of wet chemical etches also contributes to problems with device reproducibility and yield. These etches are adequate for demonstration purposes with single devices or small circuits, but would not be suitable for the ultimate goal, large-scale GaAs ICs. However, wet etches could be adequate if HJFET technology was used for GaAs power FETs. The analogous dry etch processes for GaAs, AlGaAs and other III-V compounds are currently being developed, motivated largely by the desire to process optoelectronic devices.<sup>13-16</sup> A selective etch of GaAs against AlGaAs, the analog of citric acid, seems to be an O<sub>2</sub>/CCl<sub>2</sub>F<sub>2</sub> plasma etch.<sup>13</sup> While it is known that an HF plasma will not etch GaAs,<sup>15</sup> nothing has yet been published on selective dry etching of AlGaAs against GaAs. Along with many possibilities for selective etching that have not been tried, several endpoint detection techniques are available with dry etch processes, including mass spectrometry and, in the case of reactive ion beam etching (RIBE), sputter yield current monitoring. Given the strong interest in development of dry processes for III-Vs, one can reasonably expect dry etches for the HJFET process to be available in the future.

In an HJFET integrated circuit, there is the problem of connecting to the gate metal that is atop the gate cap layer. Figure 26a shows how the problem is currently solved with the ring oscillators -- a thick layer of Al bridges the gap between gate cap and substrate. A smoother transition to the substrate, without an extra metal layer, could be arranged by using the fact that OM GaAs will grow selectively in holes in SiO<sub>2</sub>, as shown in Fig. 26b. The gates must be aligned along (100) equivalent directions (45° from the cleavage planes) in order to give the desired "ramp". This scheme also produces a grown-junction HJFET.

GaAs digital integrated circuits are at present dominated by ion implantation technologies, which offer the advantage of planar devices. Any alternate scheme must contend with this competition. The MBE pro-



a) Present method, 4000 Å Al.



b) Projected all-OM HJFET, selective growth with gates along (100).

Fig. 26 HJFET metal interconnections.

cess can be planarized by selective growth of GaAs in oxide holes, shown by experiments done at Cornell<sup>17</sup> and verified at Varian. The GaAs grows polycrystalline on the thin (250 Å) oxide and the resulting surface is nearly planar. This technique might be usable with the HJFET, depending on how the resistivity and etch properties of the poly-GaAs turned out. But the resulting circuit would not be planar, since the HJFET is fundamentally a nonplanar device.

These proposed improvements to the HJFET would likely result in better devices for ICs, but the advantages over ion-implanted ICs would be limited and the nonplanarity of the process would have to be tolerated. Because MBE and OM-VPE are capable of multiple layer growth, the nonplanarity of these devices could be extended to give a certain amount of vertical integration, resulting in circuits with higher packing density than could be achieved with ion implantation. Details are discussed in a separate document.<sup>18</sup> Given the heavy financial support for ion-implanted GaAs technologies, we feel that the future of the HJFET and related approaches will hinge on taking full advantage of its nonplanarity and of the unique capabilities of MBE and OM epitaxy. Because the industry has other incentives (e.g., optoelectronic devices) to develop the required process technologies, HJFETs or related devices could yet be seen in the GaAs integrated circuits of the future.

## REFERENCES

1. H. Morkoc et al., "Heterojunction Gate GaAs FET Study," Varian Final Report on NRL Contract N00173-76-C-0317 (1977).
2. H. Morkoc et al., "A Study of High-Speed Normally-Off and Normally-On Al<sub>.5</sub>Ga<sub>.5</sub>As Heterojunction Gate GaAs FETs (HJFET)," IEEE Trans. Elec. Dev. ED-25, 619 (1980).
3. T. J. Maloney, "Normally-Off GaAs FET Monolithic Technology," Varian Final Report on NRL Contract N00173-78-C-0104.
4. M. Otsubo et al., "Preferential Etching of GaAs through Photoresist Masks," J. Electrochem. Soc. 123, 676 (1976).
5. W. Spicer, et al., "Unified Mechanism for Schottky-Barrier Formation and III-V Oxide Interface States," Phys. Rev. B 44, 420 (1980).
6. D. Boccon-Gibod, et al., "The Use of GaAs-(Ga,Al)As Heterostructures for FET Devices," IEEE Trans. Elec. Dev. ED-27, 1141 (1980).
7. H. Morkoc, et al., "Contact Potential of p-Al<sub>.5</sub>Ga<sub>.5</sub>As/n-GaAs Structures," Sol. State Elec. 21, 663 (1978).
8. C. H. Henry, et al., "The Effect of Surface Recombination on Current in Al<sub>x</sub>Ga<sub>1-x</sub>As Heterojunctions," J. Appl. Phys. 49, 3530 (1978).
9. H. C. Casey, et al., "Reduction of Surface Recombination Current in GaAs p-n Junctions," Appl. Phys. Lett. 34, 594 (1979).
10. S. C. Lee and G. L. Pearson, "Current Reduction in Al<sub>x</sub>Ga<sub>1-x</sub>As-GaAs Heterojunction Diodes," J. Appl. Phys. 52, 275 (1981).

11. J. P. Donnelly and A. G. Milnes, "The Capacitance of p-n Heterojunctions Including the Effects of Interface States," IEEE Trans. Elec. Dev. ED-14, 63 (1967).
12. K. Lebovec and R. Zuleeg, "Analysis of GaAs FETs for Integrated Logic," IEEE Trans. Elec. Dev. ED-27, 1074 (1980).
13. C. B. Burstell, et al., "Perferential Etch Scheme for GaAs-GaAlAs," IBM Tech. Disc1. Bull. 20, 2451 (1977).
14. E. L. Hu and R. E. Howard, "Reactive-Ion Etching of GaAs and InP Using  $CCl_2F_2/Ar/O_2$ ," Appl. Phys. Lett. 37, 1022 (1980).
15. G. Smolinsky, et al., "Planar Etching of III-V Compound Semiconductor Materials and Their Oxides," J. Vac. Sci. Tech. 18, 12 (1981).
16. R. G. Klinger and J. E. Greene, "Reactive Ion Etching of GaAs in  $CCl_2F_2$ ," Appl. Phys. Lett. 38, 620 (1981).
17. G. M. Metze, et al., "GaAs Integrated Circuits by Selected-Area Molecular Beam Epitaxy," Appl. Phys. Lett. 37, 628 (1980).
18. T. J. Maloney, "Vertically Integrated GaAs JFET Logic," Varian CRM-388 (1981). Patent application in progress.

To be presented at the Device Research Conference, Santa Barbara, Cal., June 24, 1981

AlGaAs HETEROJUNCTION GATE GaAs FETs BY ORGANOMETALLIC  
AND MOLECULAR BEAM EPITAXY\*

Timothy J. Maloney  
Varian Associates, Inc.  
611 Hansen Way  
Palo Alto, CA 94303  
(415) 493-4000, Ext. 3671

AlGaAs heterojunction gate GaAs FETs (HJFETs) have been proposed for high-speed logic because of their self-aligned features and high built-in voltage, and have previously been produced by growing liquid-phase epitaxial gate layers on a mesa-etched n-GaAs active layer so that low capacitance and high-speed switching can be achieved.<sup>1</sup> This work concerns the use of organometallic vapor phase epitaxy (OM-VPE) and molecular beam epitaxy (MBE), which lead to superior results because of enhanced uniformity and reproducibility. Process steps such as a plasma ash and *in situ* heat cleaning of the mesa-etched layer before OM-VPE gate growth must be taken in order to ensure that the interface is clean and free of carbon contamination. Moreover, a very thin (200 Å) p<sup>+</sup>-GaAs layer between the n-GaAs channel and the p<sup>+</sup>-AlGaAs helps to isolate the actual p<sup>+</sup>n gate junction from oxygen that is gettered into AlGaAs grown by OM-VPE. C-V measurements indicate a 1.3V built-in voltage for this junction, while forward I-V characteristics give a nonideality factor n=2 and are similar to those of a GaAs p-n junction. Thus the electrical characteristics of the heterojunction are retained, along with the advantages of selective undercut etching and self-aligned metal.

Since normally-off HJFETs are desired for direct coupling of logic circuits, control of threshold voltage is very important. Although HJFETs with record high saturation currents were produced with buffered active layers grown by both chloride transport VPE and MBE, extremely good threshold voltage control (variations of 0.1-0.2V over a 1 cm<sup>2</sup> wafer) was achieved with MBE. Saturation currents for normally-off HJFETs followed a square law and were the highest ever observed, greater than 50 μA/μm·V<sup>2</sup> for 3 x 300 μm and 1 x 300 μm gate devices. Pt-Au gate metal, as proposed by LEP,<sup>2</sup> is especially useful for achieving self-aligned, undercut-etched 1-μm devices.

1. H. Morkoc, et. al., IEEE Trans. Elec. Dev. ED-25, 619 (1978).
2. D. Boccon-Gibod, et. al., IEEE Trans Elec. Dev. ED-27, 1141 (1980).

\*Some preliminary results were reported at the Semiconductor Interface Specialists' Conference, Dec. 1980 (abstracts not distributed).

DISTRIBUTION LIST

	<u>Copies</u>
Defense Documentation Center Bldg. 5, Cameron Station Alexandria, VA 22314	12
Advisory Group on Electron Devices 201 Varick St., 9th Floor New York, NY 10014	3
Dr. R. Burke, Code 61R NAVELEX 8E08 National Center #1 Washington, DC 20360	2
Commander Naval Air Systems Command Washington, DC 20361	
Attn: Mr. Andrew Glista, Jr., AIR 360-G	1
Mr. George B. Cudd, Jr., AIR 5162C	10
Mr. J. D. Letellier, ELEX 6142	1
Mr. Ronald A. Wade, ELEX 61421	1
ELEX 614	1
Mr. P. Lupino, AIR 360-C	1
Commanding Officer Naval Research Laboratory Washington, DC 20375	
Attn: Dr. Kenneth J. Sleger, Code 6811	1
Dr. Barry E. Spielman, Code 6851	1
Dr. Bruce McCombe, Code 6800	1
Dr. John Davey, Code 6810	10
Dr. Lawrence R. Whicker, Code 6850	1
Mr. Howard Lessoff, Code 6820	1
Mr. Alan C. Macpherson, Code 6811-M	1
Dr. C. Rauscher, Code 6851	1
Mr. Robert Neidert, Code 6851	1
Mr. T. ApRhys, Code 5366	1
Mr. W. Howell, Code 5709	1
Mr. R. Evans, Code 5753	1

Office of Naval Research  
Attn: Mr. M. N. Yoder, Code 427  
800 North Quincy Street  
Arlington, VA 22217

Reliability Analysis Center  
Rome Air Development Center  
Attn: RADC/RBRAC  
(I. L. Krulac)  
Griffiss AFB, NY 13441

Director  
Naval Weapons Center  
Attn: Mr. Sterling Haaland, Code 39012  
China Lake, CA 93555

Director of Defense Research  
and Engineering  
Attn: Tech Library  
Rm. 3E 1039, The Pentagon  
Washington, DC 20301

Director  
Pacific Missile Test Center  
Attn: Mr. John Hurley, Code 1151  
Point Mugu, CA 93042

Defense Advanced Research  
Projects Agency  
Attn: Dr. Richard Reynolds  
1400 Wilson Blvd.  
Arlington, VA 22309

Commander  
Naval Air Development Center  
Attn: Dr. John K. Smith, Code 3022  
Warminster, PA 18974

Director  
US Army Ballistic Missile Defense  
Advanced Technology Center  
Attn: ATC-R, Mr. G. Jones  
P. O. Box 1500  
Huntsville, AL 35807

Commander  
Naval Electronic Systems Command  
NAVELEX 350  
Washington, DC 20360

NASA-Goddard Space Flight Center  
Attn: Mr. Dominick E. Santarpia  
Code 763  
Greenbelt, MD 20771

Commander  
Naval Sea Systems Command  
NAVSEA 652  
Washington, DC 20362

NASA-Lewis Research Center  
Attn: Mr. Robert E. Alexovich  
Code 6230  
Cleveland, OH 44135

Commander  
Naval Ocean Systems Center  
Attn: Library  
297 Catalina Blvd.  
San Diego, CA 92152

Dr. H. Walter Cox  
Georgia Institute of Technology  
Engineering Experiment Station  
Atlanta, GA 30332

Commanding Officer  
Harry Diamond Laboratories  
Advanced Research Laboratory  
Attn: Mr. R. L. Remski, AFAL/DHM  
Wright-Patterson AFB, OH 45433

Dr. George I. Haddad  
University of Michigan  
Electrical Engrg. Dept.  
Ann Arbor, MI 48104

Commander  
U.S. Army ERADCOM  
Fort Monmouth, NJ 07703

Attn: DELET-M, Mr. V. C. Gelnovatch  
DELET-MK, Mr. R. A. Weck

Commander  
Air Force Avionics Laboratory  
Wright Patterson AFB, OH 45433

Attn: Mr. R. L. Remski, AFAL/DHM  
Mr. Chern Huang, AFAL/DHM

Cornell University  
Electrical Engineering Dept.  
Phillips Hall  
Ithaca, NY 14850

Attn: Dr. Walter Ku  
Dr. Lester Eastman  
Dr. Jeffrey Frey

AI  
Attn: Mr. Joseph D. Rella  
Melville, LI, NY 11746

AILTECH  
Attn: Dr. George D. Vendelin  
612 North Mary Ave.  
Sunnyvale, CA 94086

Avantek  
Attn: Dr. R. M. Malbon  
3175 Bowers Ave.  
Santa Clara, CA 95051

Hughes Aircraft Company  
3100 West Lomita Blvd.  
Torrance, CA 90509

Attn: Dr. J. Schellenberg  
Dr. T. Midford

Microwave Associates  
Attn: Dr. Joseph A. Saloom  
Northwest Industrial Park  
Burlington, MA 01803

Raytheon Company  
Attn: Dr. Robert Pucel  
28 Seyon Street  
Waltham, MA 02154

Raytheon Company  
Attn: Dr. B. Hewett  
130 Second Avenue  
Waltham, MA 02154

Rockwell International Science Center  
Attn: Dr. F. Eisen  
1049 Camino Dos Rios (Box 1085)  
Thousand Oaks, CA 91360

Avantek  
Attn: Mr. R. Dyafuss  
3175 Bowers Ave.  
Santa Clara, CA 95051

Bell Telephone Laboratories  
Attn: Dr. J. V. DiLorenzo  
600 Mountain Ave.  
Murray Hill, NJ 07974

E Systems Inc.  
Attn: Mr. S. March  
Unit 50280  
Box 226118  
Dallas, TX 75266

Hewlett-Packard, Inc.  
Attn: Dr. C. Liechti  
1501 Page Mill Road  
Palo Alto, CA 94304

Hughes Aircraft Company  
Attn: Dr. C. Krumm  
3011 Malibu Canyon Rd  
Malibu, CA 90265

Hughes Aircraft Co.  
Attn: Dr. R. L. Eisenhart  
Canoga Park, CA 91304

Microwave Semiconductor Corp.  
Attn: Dr. Ira Drukier  
100 Schoolhouse Road  
Somerset, NJ 08873

Raytheon Company  
Attn: Mr. R. Sparks  
Mail Stop CS 2-58  
Bedford, MA 01730

Raytheon  
Attn: Mr. R. Rose  
138 Kifer Court  
Sunnyvale, CA 94086

RCA  
David Sarnoff Research Center  
Princeton, NJ 08540  
Attn: Dr. F. Steizer  
Dr. Y. Narayan  
Mr. H. Wolkstein

Teledyne/MEC  
3165 Porter Drive  
Palo Alto, CA 94304

Attn: Mr. Frank Emery  
Dr. Martin Grace

Teledyne Ryan Electronics  
Attn: Mr. Gerald Schaffner  
2701 Harbor Drive  
San Diego, CA 92112

TRW  
One Space Park  
Redondo Beach, CA 90278

Attn: Dr. T. Mills  
Mr. Dale Claxton  
Mr. B. Copeland

Varian Associates, Inc.  
Attn: Mr. H. Cooke  
3251 Olcott Street  
Santa Clara, CA 95050

Watkins-Johnson Company  
3333 Hillview Avenue  
Palo Alto, CA 94304

Attn: Dr. E. J. Crescenzi, Jr.  
Dr. K. Niclas

Tektronix  
Attn: Mr. Philip B. Snow  
M/S 58-733, Box 500  
Beaverton, OR 97077

Westinghouse Research Laboratories  
Attn: Dr. H. C. Nathanson  
Beulah Road  
Pittsburgh, PA 15235

Westinghouse Electric Corp.  
Attn: Dr. W. Cooper  
Box 746  
Baltimore, MD 21203

END

DATE

FILMED

8 - 81

DTIC